

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90570/A Series

MB90573/574/F574/V570/574A/F574A/V570A

■ DESCRIPTION

The MB90570/A series is a general-purpose 16-bit microcontroller developed and designed by Fujitsu for process control applications in consumer products that require high-speed real time processing. It contains an I²C*² bus interface that allows inter-equipment communication to be implemented readily. This product is well adapted to car audio equipment, VTR systems, and other equipment and systems.

The instruction set of F²MC-16LX CPU core inherits AT architecture of F²MC*¹ family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

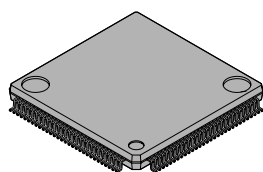
The MB90570/A series has peripheral resources of an 8/10-bit A/D converter, an 8-bit D/A converter, UART (SCI), an extended I/O serial interface, an 8/16-bit up/down counter/timer, an 8/16-bit PPG timer, I/O timer (a 16-bit free run timer, an input capture (ICU), an output compare (OCU)).

*1: F²MC stands for FUJITSU Flexible Microcontroller.

*2: Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

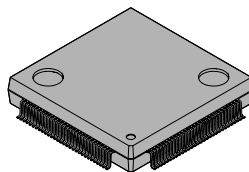
■ PACKAGE

120-pin plastic LQFP



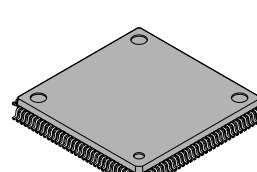
(FPT-120P-M05)

120-pin plastic QFP



(FPT-120P-M13)

120-pin plastic LQFP



(FPT-120P-M21)

MB90570/A Series

■ FEATURES

- Clock
 - Embedded PLL clock multiplication circuit
 - Operating clock (PLL clock) can be selected from 1/2 to 4× oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
 - Minimum instruction execution time : 62.5 ns (at oscillation of 4 MHz, 4× PLL clock, operation at V_{CC} of 5.0 V)
- Maximum memory space
 - 16 Mbytes
- Instruction set optimized for controller applications
 - Rich data types (bit, byte, word, long word)
 - Rich addressing mode (23 types)
 - Enhanced signed multiplication/division instruction and RETI instruction functions
 - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
 - Adoption of system stack pointer
 - Enhanced pointer indirect instructions
 - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed
 - 4-byte instruction queue
- Enhanced interrupt function
 - 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
 - Extended intelligent I/O service function (EI²OS): Up to 16 channels
- Embedded ROM size and types
 - Mask ROM: 128 Kbytes/256 Kbytes
 - Flash ROM: 256 Kbytes
 - Embedded RAM size: 6 Kbytes/10 Kbytes (mask ROM)
 - 10 Kbytes (flash memory)
 - 10 Kbytes (evaluation device)
- Low-power consumption (standby) mode
 - Sleep mode (mode in which CPU operating clock is stopped)
 - Stop mode (mode in which oscillation is stopped)
 - CPU intermittent operation mode
 - Hardware standby mode
- Process
 - CMOS technology
- I/O port
 - General-purpose I/O ports (CMOS): 63 ports
 - General-purpose I/O ports (with pull-up resistors): 24 ports
 - General-purpose I/O ports (open-drain): 10 ports
 - Total: 97 ports

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MB90570/A Series

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- Timer
 - Timebase timer/watchdog timer: 1 channel
 - 8/16-bit PPG timer: 8-bit × 2 channels or 16-bit × 1 channel
- 8/16-bit up/down counter/timer: 1 channel (8-bit × 2 channels)
- 16-bit I/O timer
 - 16-bit free run timer: 1 channel
 - Input capture (ICU): Generates an interrupt request by latching a 16-bit free run timer counter value upon detection of an edge input to the pin.
 - Output compare (OCU): Generates an interrupt request and reverse the output level upon detection of a match between the 16-bit free run timer counter value and the compare setting value.
- Extended I/O serial interface: 3 channels
- I²C interface (1 channel)
 - Serial I/O port for supporting Inter IC BUS
- UART0 (SCI), UART1 (SCI)
 - With full-duplex double buffer
 - Clock asynchronized or clock synchronized transmission can be selectively used.
- DTP/external interrupt circuit (8 channels)
 - A module for starting extended intelligent I/O service (EI²OS) and generating an external interrupt triggered by an external input.
- Delayed interrupt generation module
 - Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
 - 8/10-bit resolution
 - Starting by an external trigger input.
 - Conversion time: 26.3 μs
- 8-bit D/A converter (based on the R-2R system)
 - 8-bit resolution: 2 channels (independent)
 - Setup time: 12.5 μs
- Clock timer: 1 channel
- Chip select output (8 channels)
 - An active level can be set.
- Clock output function

MB90570/A Series

■ PRODUCT LINEUP

<div>Part number</div> <div>Item</div>		MB90573	MB90574/A	MB90F574/A	MB90V570/A
Classification		Mask ROM products		Flash ROM products	Evaluation product
ROM size		128 Kbytes	256 Kbytes		None
RAM size		6 Kbytes	10 Kbytes		
CPU functions		The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock of 16 MHz, minimum value)			
Ports		General-purpose I/O ports (CMOS output): 63 General-purpose I/O ports (with pull-up resistor): 24 General-purpose I/O ports (N-ch open-drain output): 10 Total: 97			
UART0 (SCI), UART1 (SCI)		Clock synchronized transmission (62.5 kbps to 1 Mbps) Clock asynchronized transmission (1202 bps to 9615 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.			
8/10-bit A/D converter		Resolution: 8/10-bit Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Scan conversion mode (converts two or more successive channels and can program up to 8 channels.) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)			
8/16-bit PPG timer		Number of channels: 1 (or 8-bit × 2 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: 62.5 ns to 1 μs (at oscillation of 4 MHz, machine clock of 16 MHz)			
8/16-bit up/down counter/timer		Number of channels: 1 (or 8-bit × 2 channels) Event input: 6 channels 8-bit up/down counter/timer used: 2 channels 8-bit re-load/compare function supported: 1 channel			
16-bit I/O timer	16-bit free run timer	Number of channel: 1 Overflow interrupts			
	Output compare (OCU)	Number of channels: 4 Pin input factor: A match signal of compare register			
	Input capture (ICU)	Number of channels: 2 Rewriting a register value upon a pin input (rising, falling, or both edges)			

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MB90570/A Series

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Part number Item	MB90573	MB90574/A	MB90F574/A	MB90V570/A
DTP/external interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input. External interrupt circuit or extended intelligent I/O service (EI ² OS) can be used.			
Delayed interrupt generation module	An interrupt generation module for switching tasks used in real time operating systems.			
Extended I/O serial interface	Clock synchronized transmission (3125 bps to 1 Mbps) LSB first/MSB first			
I ² C interface	Serial I/O port for supporting Inter IC BUS			
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)			
8-bit D/A converter	8-bit resolution Number of channels: 2 channels Based on the R-2R system			
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)			
Low-power consumption (standby) mode	Sleep/stop/CPU intermittent operation/clock timer/hardware standby			
Process	CMOS			
Power supply voltage for operation*	4.5 V to 5.5 V			

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

Assurance for the MB90V570/A is given only for operation with a tool at a power voltage of 4.5 V to 5.5 V, an operating temperature of 0 to +25°C, and an operating frequency of 1 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90573	MB90574	MB90F574/A	MB90574A
FPT-120P-M05	○	○	○	×
FPT-120P-M13	○	○	○	○
FPT-120P-M21	×	×	○	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

MB90570/A Series

■ DIFFERENCES AMONG PRODUCTS

Memory Size

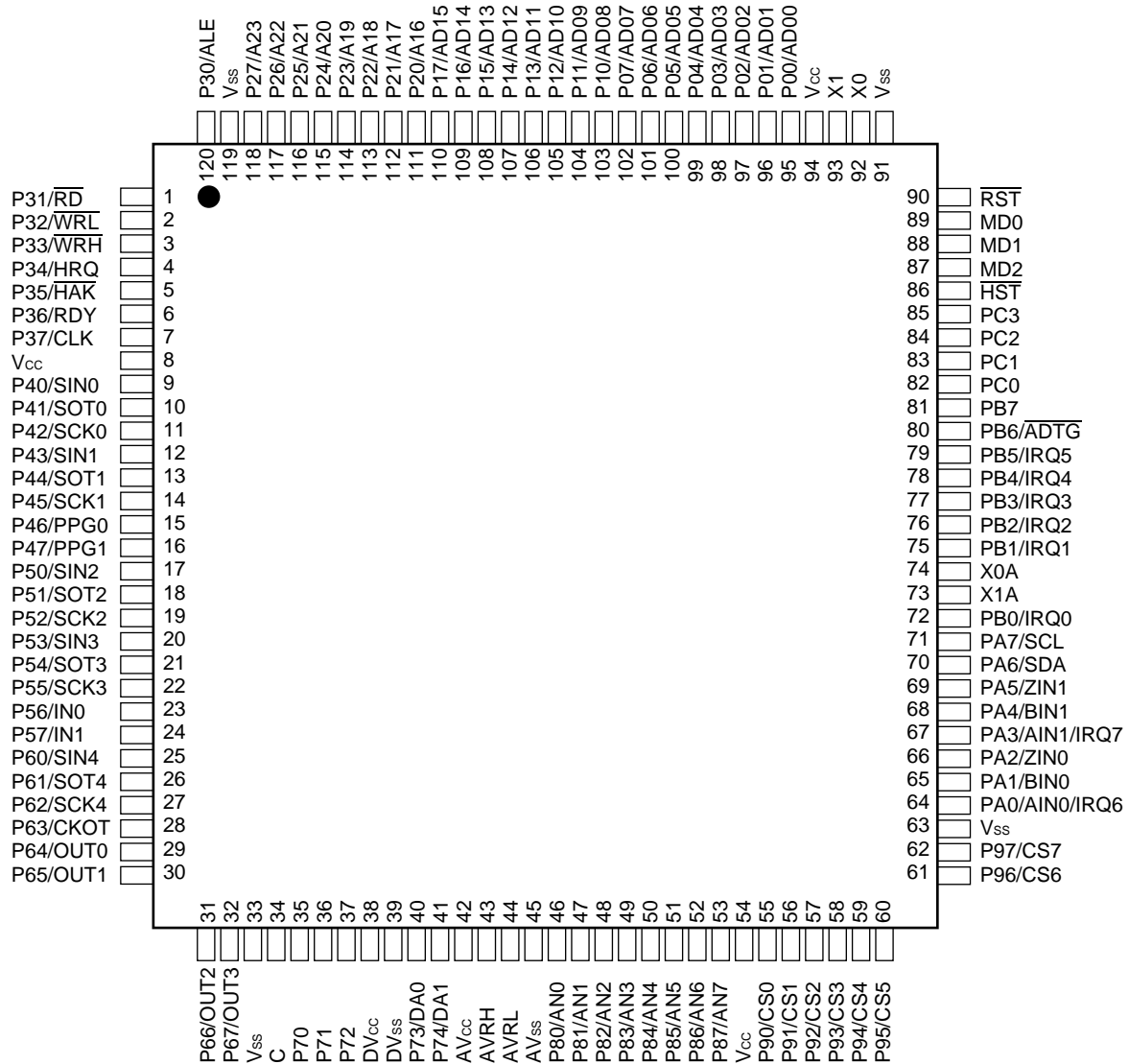
In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V570/A does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V570/A, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FE0000_H to FF3FFF_H to mapped to bank FE and FF only. (This setting can be changed by configuring the deveolpment tool.)
- In the MB90F574/574/573/F574A/574A, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FF0000_H to FF3FFF_H to bank FF only.
- The products designated with /A are different from those without /A in that they are DTP/externally-interrupted types which return from standby mode at the ch.0 to ch.1 edge request.

MB90570/A Series

PIN ASSIGNMENT

(Top view)



(FPT-120P-M05)
 (FPT-120P-M13)
 (FPT-120P-M21)

MB90570/A Series

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
LQFP-120 *1 QFP-120 *2			
92,93	X0,X1	A	High speed oscillator input pins
74,73	X0A,X1A	B	Low speed oscillator input pins
89 to 87	MD0 to MD2	C	These are input pins used to designate the operating mode. They should be connected directly to Vcc or Vss.
90	$\overline{\text{RST}}$	C	Reset input pin
86	$\overline{\text{HST}}$	C	Hardware standby input pin
95 to 102	P00 to P07	D	In single chip mode, these are general purpose I/O pins. When set for input, they can be set by the pull-up resistance setting register (RDR0). When set for output, this setting will be invalid.
	AD00 to AD07		In external bus mode, these pins function as address low output/data low I/O pins.
103 to 110	P10 to P17	D	In single chip mode, these are general purpose I/O pins. When set for input, they can be set by the pull-up resistance setting register (RDR1). When set for output, the setting will be invalid.
	AD08 to AD15		In external bus mode, these pins function as address middle output/data high I/O pins.
111 to 118	P20 to P27	E	In single chip mode this is a general-purpose I/O port.
	A16 to A23		In external bus mode, these pins function as address high output pins.
120	P30	E	In single chip mode this is a general-purpose I/O port.
	ALE		In external bus mode, this pin functions as the address latch enable signal output pin.
1	P31	E	In single chip mode this is a general-purpose I/O port.
	$\overline{\text{RD}}$		In external bus mode, this pin functions as the read strobe signal output pin.
2	P32	E	In single chip mode this is a general-purpose I/O port.
	$\overline{\text{WRL}}$		In external bus mode, this pin functions as the data bus lower 8-bit write strobe signal output pin.
3	P33	E	In single chip mode this is a general-purpose I/O port..
	$\overline{\text{WRH}}$		In external bus mode, this pin functions as the data bus upper 8-bit write strobe signal output pin.
4	P34	E	In single chip mode this is a general-purpose I/O port.
	HRQ		In external bus mode, this pin functions as the hold request signal input pin.
5	P35	E	In single chip mode this is a general-purpose I/O port.
	$\overline{\text{HAK}}$		In external bus mode, this pin functions as the hold acknowledge signal output pin.
6	P36	E	In single chip mode this is a general-purpose I/O port.
	RDY		In external bus mode, this pin functions as the ready signal input pin.

*1: FPT-120P-M05

*2: FPT-120P-M13,FPT-120P-M21

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MB90570/A Series

Pin no. LQFP-120 *1 QFP-120 *2	Pin name	Circuit type	Function
7	P37	E	In single chip mode this is a general-purpose I/O port.
	CLK		In external bus mode, this pin functions as the clock (CLK) signal output pin.
9	P40	F	In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register.
	SIN0		This is also the UART ch.0 serial data input pin. While UART ch.0 is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed. If shared by output from other functions, this pin should be output disabled during SIN operation.
10	P41	F	In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register.
	SOT0		This is also the UART ch.0 serial data output pin. This function is valid when UART ch.0 is enabled for data output.
11	P42	F	In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register.
	SCK0		This is also the UART ch.0 serial clock I/O pin. This function is valid when UART ch.0 is enabled for clock output.
12	P43	F	In single chip mode this is a general-purpose I/O port. It can be set to open-drain by the ODR4 register.
	SIN1		This is also the UART ch.1 serial data input pin. While UART ch.1 is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed. If shared by output from other functions, this pin should be output disabled during SIN operation.
13	P44	F	In single chip mode this is a general-purpose I/O port. It can be set to opendrain by the ODR4 register.
	SOT1		This is also the UART ch.1 serial data output pin. This function is valid when UART ch.1 is enabled for data output.
14	P45	F	In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register.
	SCK1		This is also the UART ch.1 serial clock I/O pin. This function is valid when UART ch.1 is enabled for clock output.
15,16	P46,P47	F	In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register.
	PPG0,PPG1		These are also the PPG0, 1 output pins. This function is valid when PPG0, 1 output is enabled.
17	P50	E	In single chip mode this is a general-purpose I/O port.
	SIN2		This is also the I/O serial ch.0 data input pin. During serial data input, this input signal is in continuous use, and therefore the output function should only be used when needed.

*1: FPT-120P-M05

(Continued)

*2: FPT-120P-M13,FPT-120P-M21

MB90570/A Series

Pin no.	Pin name	Circuit type	Function
LQFP-120 *1 QFP-120 *2			
18	P51	E	In single chip mode this is a general-purpose I/O port.
	SOT2		This is also the I/O serial ch.0 data output pin. This function is valid when serial ch.0 is enabled for serial data output.
19	P52	E	In single chip mode this is a general-purpose I/O port .
	SCK2		This is also the I/O serial ch.0 clock I/O pin. This function is valid when serial ch.0 is enabled for serial data output.
20	P53	E	In single chip mode this is a general-purpose I/O port.
	SIN3		This is also the I/O serial ch.1 data input pin. During serial data input, this input signal is in continuous use, and therefore the output function should only be used when needed.
21	P54	E	In single chip mode this is a general-purpose I/O port.
	SOT3		This is also the I/O serial ch.1 data output pin. This function is valid when serial ch.1 is enabled for serial data output.
22	P55	E	In single chip mode this is a general-purpose I/O port.
	SCK3		This is also the I/O serial ch.1 clock I/O pin. This function is valid when serial ch.1 is enabled for serial data output.
23,24	P56,P57	E	In single chip mode this is a general-purpose I/O port.
	IN0,IN1		These are also the input capture ch.0/1 trigger input pins. During input capture signal input on ch.0/1 this function is in continuous use, and therefore the output function should only be used when needed.
25	P60	F	In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid.
	SIN4		This is also the I/O serial ch.2 data input pin. During serial data input this function is in continuous use, and therefore the output function should only be used when needed.
26	P61	F	In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid.
	SOT4		This is also the I/O serial ch.2 data output pin. This function is valid when serial ch.2 is enabled for serial data output.
27	P62	F	In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid.
	SCK4		This is also the I/O serial ch.2 serial clock I/O pin. This function is valid when serial ch.2 is enabled for serial data output.
28	P63	F	In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid.
	CKOT		This is also the clock monitor output pin. This function is valid when clock monitor output is enabled.

*1: FPT-120P-M05

*2: FPT-120P-M13,FPT-120P-M21

(Continued)

MB90570/A Series

Pin no.	Pin name	Circuit type	Function
LQFP-120 *1 QFP-120 *2			
29 to 32	P64 to P67	F	In single chip mode these are general-purpose I/O ports. When set for input they can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid.
	OUT0 to OUT3		These are also the output compare ch.0 to ch.3 event output pins. This function is valid when the respective channel(s) are enabled for output.
35 to 37	P70 to P72	E	These are general purpose I/O ports.
40,41	P73,P74	I	These are general purpose I/O ports.
	DA0,DA1		These are also the D/A converter ch.0,1 analog signal output pins.
46 to 53	P80 to P87	K	These are general purpose I/O ports.
	AN0 to AN7		These are also A/D converter analog input pins. This function is valid when analog input is enabled.
55 to 62	P90 to P97	E	These are general purpose I/O ports.
	CS0 to CS7		These are also chip select signal output pins. This function is valid when chip select signal output is enabled.
34	C	G	This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 μ F ceramic capacitor. Note that this is not required on the FLASH model (MB90F574/A) and MB90574A.
64	PA0	E	This is a general purpose I/O port.
	AIN0		This pin is also used as count clock A input for 8/16-bit up-down counter ch.0.
	IRQ6		This pin can also be used as interrupt request input ch. 6.
65	PA1	E	This is a general purpose I/O port.
	BIN0		This pin is also used as count clock B input for 8/16-bit up-down counter ch.0.
66	PA2	E	This is a general purpose I/O port.
	ZIN0		This pin is also used as count clock Z input for 8/16-bit up-down counter ch.0.
67	PA3	E	This is a general purpose I/O port.
	AIN1		This pin is also used as count clock A input for 8/16-bit up-down counter ch.1.
	IRQ7		This pin can also be used as interrupt request input ch.7.
68	PA4	E	This is a general purpose I/O port.
	BIN1		This pin is also used as count clock B input for 8/16-bit up-down counter ch.1.
69	PA5	E	This is a general purpose I/O port.
	ZIN1		This pin is also used as count clock Z input for 8/16-bit up-down counter ch.1.

*1: FPT-120P-M05

*2: FPT-120P-M13,FPT-120P-M21

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MB90570/A Series

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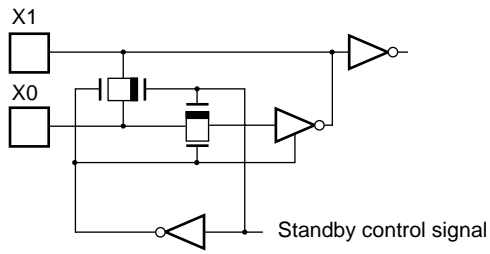
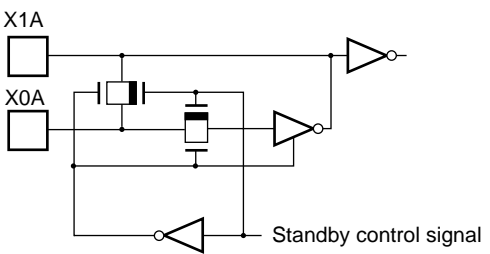
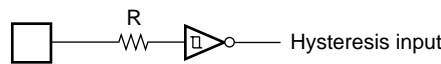
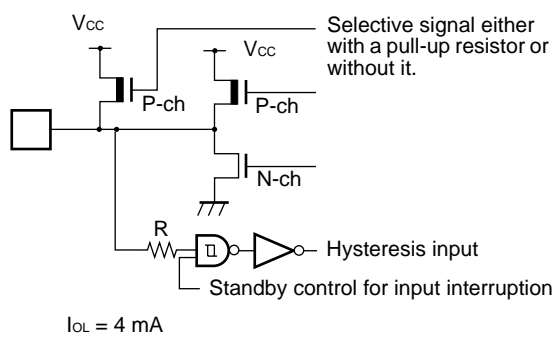
Pin no.	Pin name	Circuit type	Function
LQFP-120 *1 QFP-120 *2			
70	PA6	L	This is a general purpose I/O port.
	SDA		This pin is also used as the data I/O pin for the 1 ² C interface. This function is valid when the 1 ² C interface is enabled for operation. While the 1 ² C interface is operating this port's output level should be set to Hi-Z level (high impedance setting: PDRA=1).
71	PA7	L	This is a general purpose I/O port.
	SCL		This pin is also used as the clock I/O pin for the 1 ² C interface. This function is valid when the 1 ² C interface is enabled for operation. While the 1 ² C interface is operating this port's output level should be set to Hi-Z level (high impedance setting: PDRA=1).
72, 75 to 79	PB0, PB1 to PB5	E	These are general-purpose I/O ports.
	IRQ0, IRQ1 to IRQ5		These pins are also the external interrupt input pins. IRQ0, 1 are enabled for both rising and falling edge detection, and therefore cannot be used for recovery from STOP status for MB90V570, MB90F574, MB90573 and MB90574. However, IRQ0, 1 can be used for recovery from STOP status for MB90V570A, MB90F574A and MB90574A.
80	PB6	E	This is a general purpose I/O port.
	ADTG		This is also the A/D converter external trigger input pin. While the A/D converter is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed.
81	PB7	E	This is a general purpose I/O port.
82 to 85	PC0 to PC3	E	These are general purpose I/O ports.
8,54,94	V _{CC}	Power supply	These are power supply (5V) input pins.
33,63, 91,119	V _{SS}	Power supply	These are power supply (0V) input pins.
42	AV _{CC}	H	This is the analog macro (D/A, A/D etc.) V _{CC} power supply input pin.
43	AVRH	J	This is the A/D converter V _{ref} + input pin. The input voltage should not exceed V _{CC} .
44	AVRL	H	This is the A/D converter V _{ref} -input pin. The input voltage should not be lower than V _{SS} .
45	AV _{SS}	H	This is the analog macro (D/A, A/D etc.) V _{SS} power supply input pin.
38	DV _{CC}	H	This is the D/A converter V _{ref} input pin. The input voltage should not exceed V _{CC} .
39	DV _{SS}	H	This is the D/A converter GND power supply pin. It should be set to V _{SS} equivalent potential.

*1: FPT-120P-M05

*2: FPT-120P-M13,FPT-120P-M21

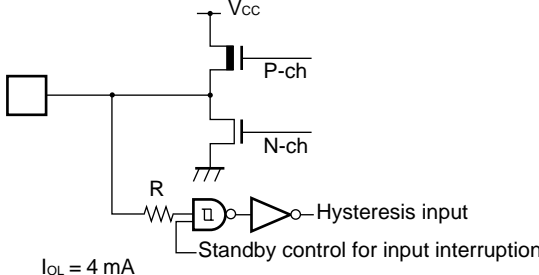
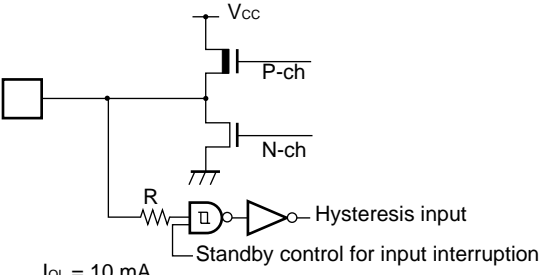
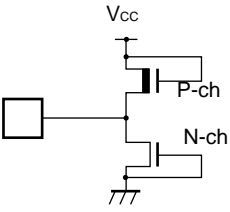
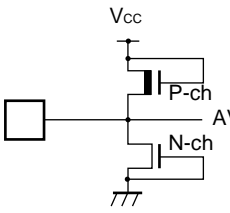
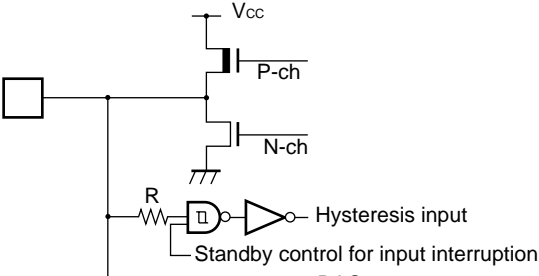
MB90570/A Series

I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> Oscillator circuit Oscillator recovery resistance for high speed= approx. $1\text{M}\Omega$
B		<ul style="list-style-type: none"> Oscillator circuit Oscillator recovery resistance for low speed =approx. $1\text{M}\Omega$
C		<ul style="list-style-type: none"> Hysteresis input pin Resistance value=approx. $50\text{k}\Omega(\text{typ.})$
D	 <p>$I_{OL} = 4\text{ mA}$</p>	<ul style="list-style-type: none"> CMOS hysteresis input pin with input pull-up control CMOS level output. CMOS hysteresis input (Includes input shutoff standby control function) Pull-up resistance value= approx.$50\text{k}\Omega(\text{typ.})$ $I_{OL} = 4\text{mA}$

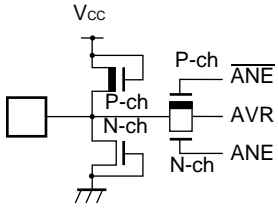
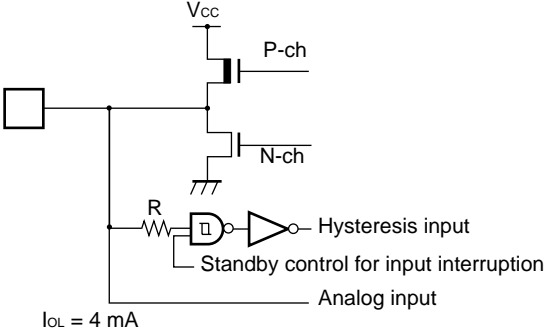
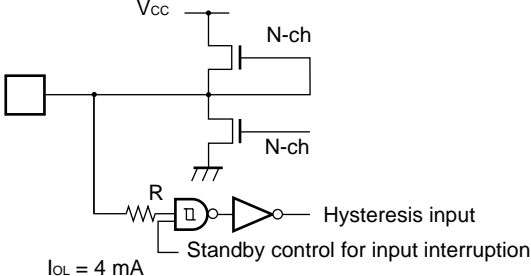
(Continued)

MB90570/A Series

Type	Circuit	Remarks
E	 <p>$I_{OL} = 4 \text{ mA}$</p>	<ul style="list-style-type: none"> CMOS hysteresis input/output pin. CMOS level output CMOS hysteresis input (Includes input shutoff standby control function) $I_{OL} = 4 \text{ mA}$
F	 <p>$I_{OL} = 10 \text{ mA}$</p>	<ul style="list-style-type: none"> CMOS hysteresis input/output pin. CMOS level output CMOS hysteresis input (Includes input shutoff standby control function) $I_{OL} = 10 \text{ mA}$ (Large current port)
G		<ul style="list-style-type: none"> C pin output (capacitance connector pin). On the MB90F574 this pin is not connected (NC).
H		<ul style="list-style-type: none"> Analog power supply protector circuit.
I	 <p>$I_{OL} = 4 \text{ mA}$</p>	<ul style="list-style-type: none"> CMOS hysteresis input/output Analog output/CMOS output dual-function pin (CMOS output is not available during analog output.) (Analog output priority : DAE = 1) Includes input shutoff standby control function. $I_{OL} = 4 \text{ mA}$

(Continued)

MB90570/A Series

Type	Circuit	Remarks
J		<ul style="list-style-type: none"> A/D converter ref+ power supply input pin(AVRH), with power supply protector circuit.
K		<ul style="list-style-type: none"> CMOS hysteresis input /analog input dual-function pin. CMOS output Includes input shutoff function at input shutoff standby.
L		<ul style="list-style-type: none"> Hysteresis input N-ch open-drain output Includes input shutoff standby control function. <p>$I_{OL} = 4\text{mA}$</p>

MB90570/A Series

■ HANDLING DEVICES

1. Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS} .

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC} , $AVRH$, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

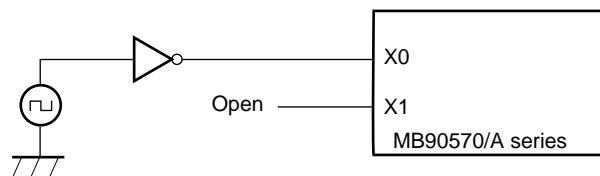
2. Connection of Unused Pins

Leaving unused pins open may result in abnormal operations. Clamp the pin level by connecting it to a pull-up or a pull-down resistor.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

• Using external clock



4. Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level and abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pin near the device.

5. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

MB90570/A Series

6. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply (AV_{CC} , $AVRH$, $AVRL$, DV_{CC} , DV_{SS}) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter and those of D/A converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

8. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

9. Notes on Energization

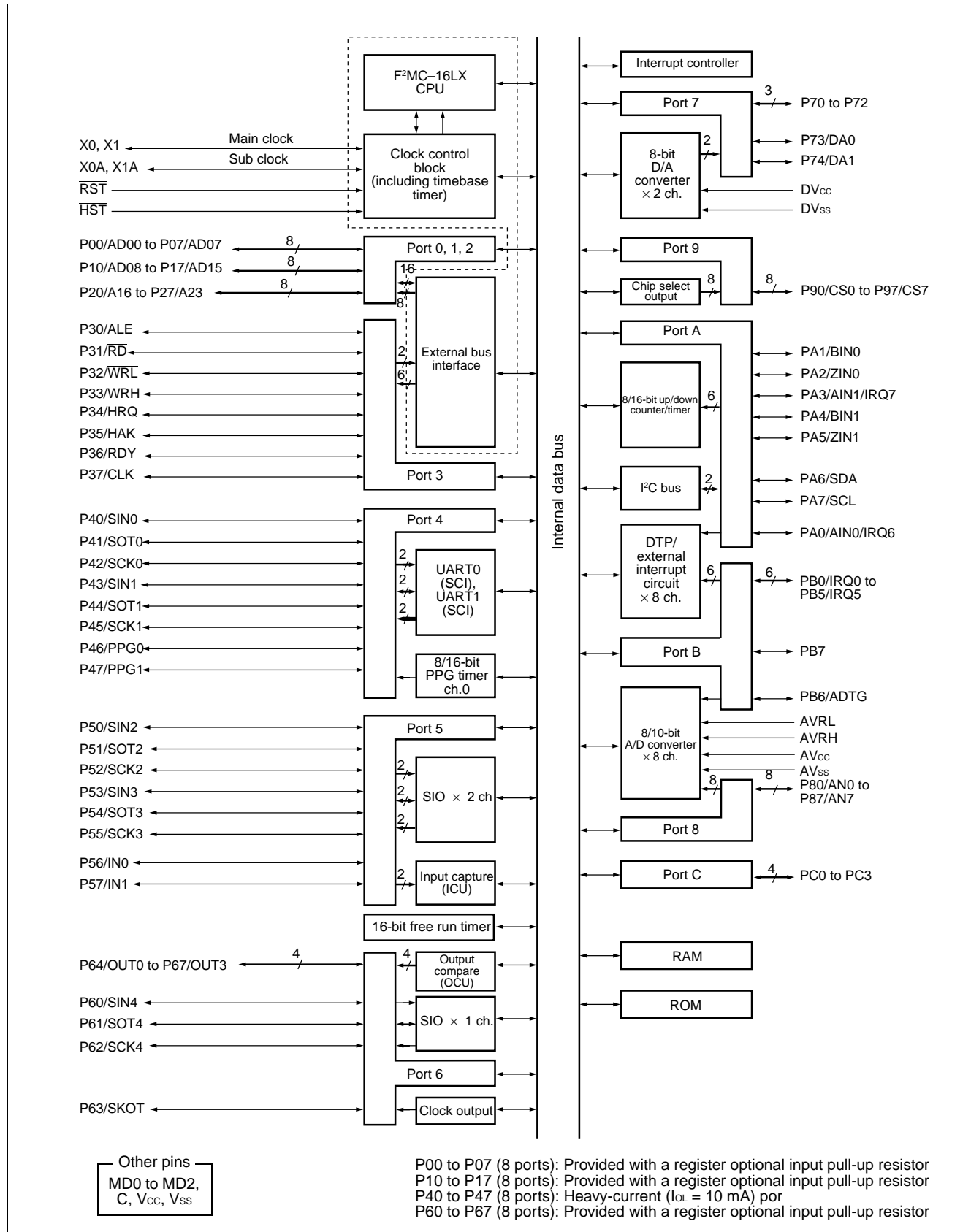
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more μs (0.2 V to 2.7 V).

10. Initialization

In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers turning on the power again.

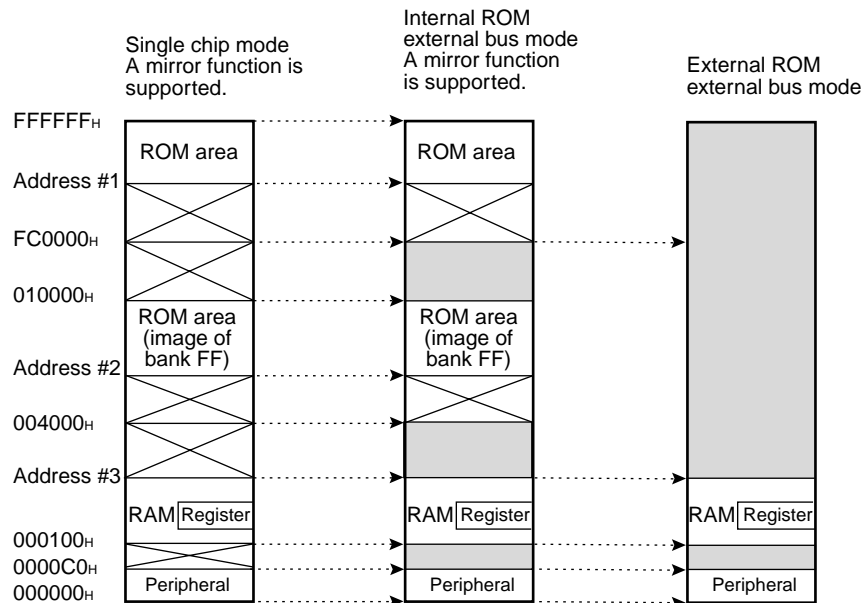
MB90570/A Series

■ BLOCK DIAGRAM



MB90570/A Series

■ MEMORY MAP



Part number	Address #1*	Address #2*	Address #3*
MB90573	FE0000H	004000H	001800H
MB90574/A	FC0000H	004000H	002900H
MB90F574/A	FC0000H	004000H	002900H

- : Internal access memory
- : External access memory
- ⊗ : Inhibited area

*: Addresses #1, #2 and #3 are unique to the product type.

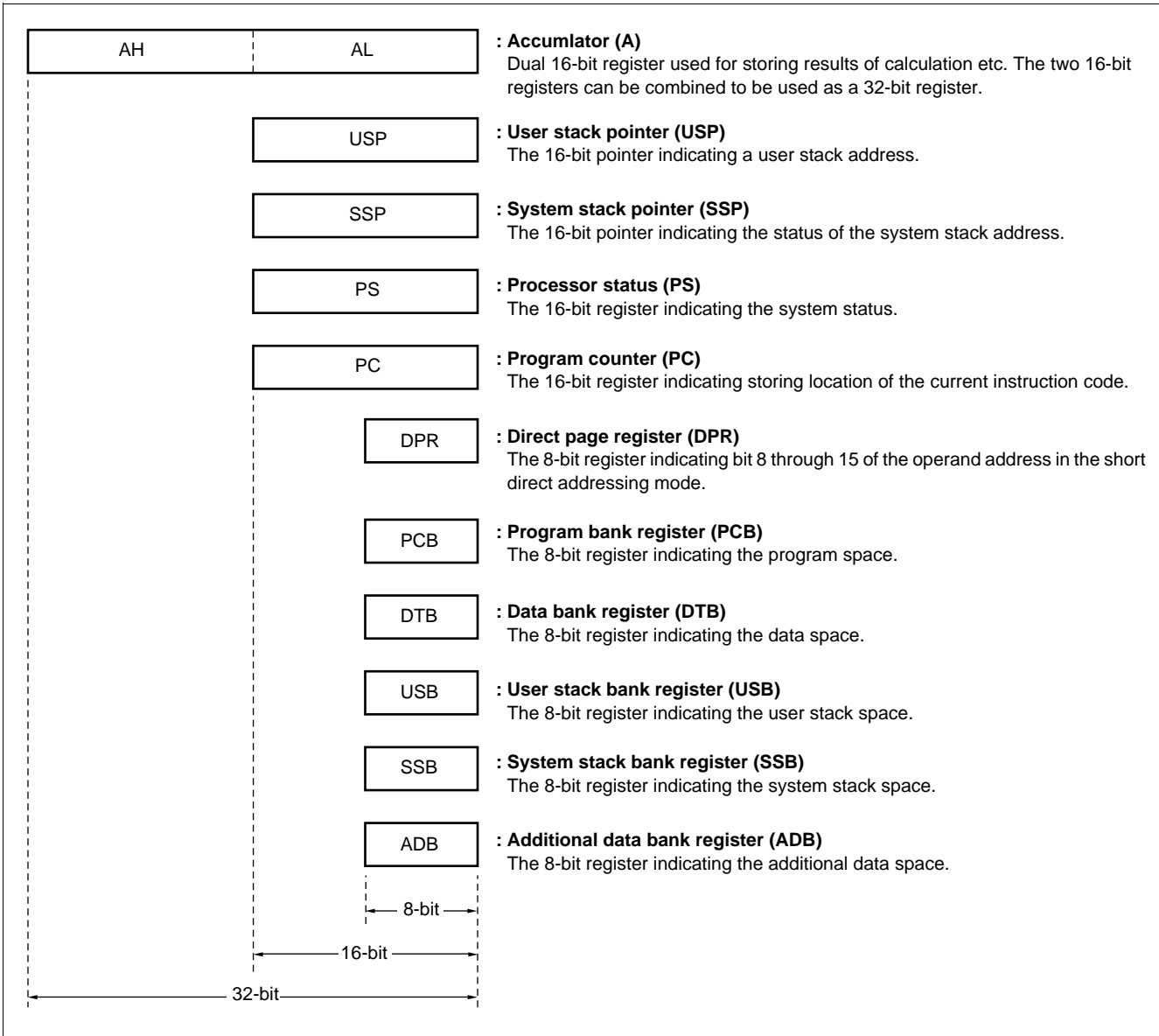
Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 is assigned to the same address, enabling reference of the table on the ROM without stating "far".

For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFFH looks, therefore, as if it were the image for 00400H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFFH.

MB90570/A Series

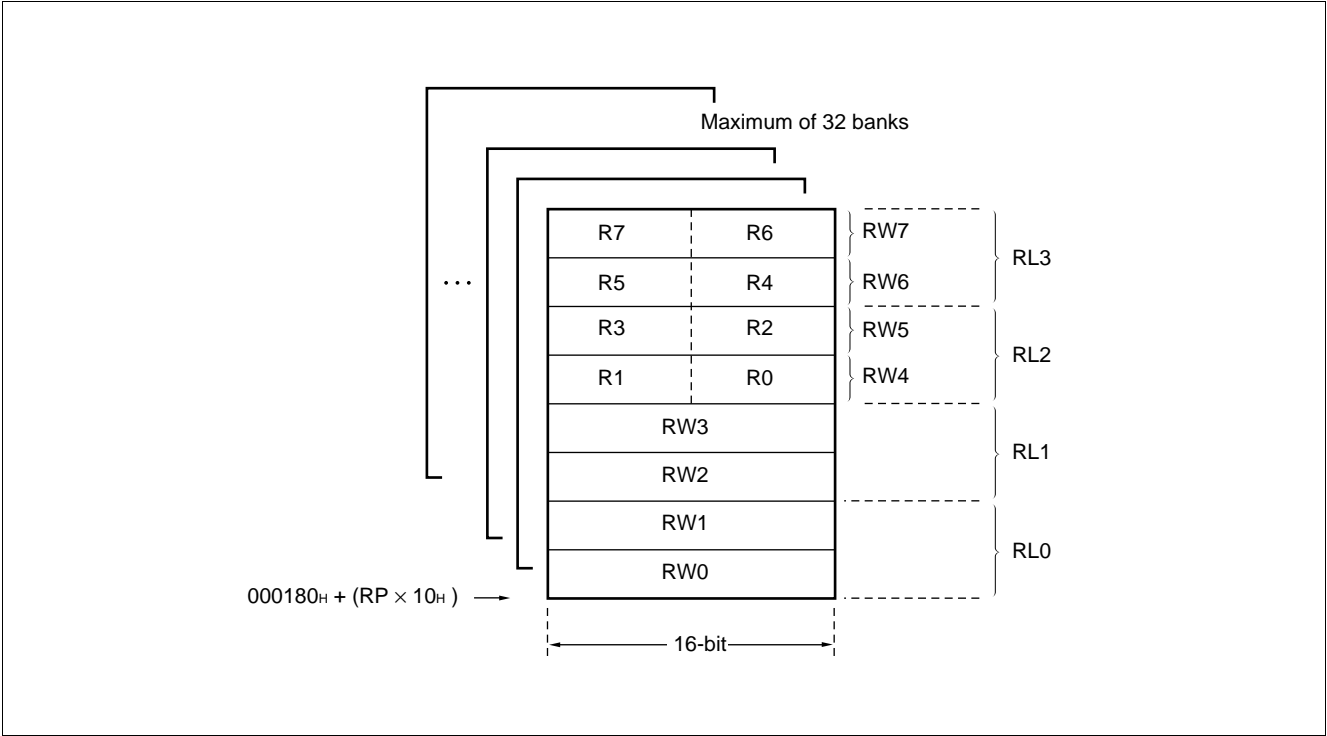
■ F²MC-16LX CPU PROGRAMMING MODEL

• Dedicated registers



MB90570/A Series

• General-purpose registers



• Processor status (PS)

ILM				RP				CCR							
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ILM2	ILM1	ILM0	B4	B3	B2	B1	B0	—	I	S	T	N	Z	V	C
Initial value	0	0	0	0	0	0	0	0	—	0	1	X	X	X	X

— : Reserved
X : Undefined

MB90570/A Series

■ I/O MAP

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000000 _H	PDR0	Port 0 data register	R/W	Port 0	X X X X X X X X _B
000001 _H	PDR1	Port 1 data register	R/W	Port 1	X X X X X X X X _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	X X X X X X X X _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	X X X X X X X X _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	X X X X X X X X _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	X X X X X X X X _B
000006 _H	PDR6	Port 6 data register	R/W	Port 6	X X X X X X X X _B
000007 _H	PDR7	Port 7 data register	R/W	Port 7	— — — X X X X X _B
000008 _H	PDR8	Port 8 data register	R/W	Port 8	X X X X X X X X _B
000009 _H	PDR9	Port 9 data register	R/W	Port 9	X X X X X X X X _B
00000A _H	PDRA	Port A data register	R/W	Port A	X X X X X X X X _B
00000B _H	PDRB	Port B data register	R/W	Port B	X X X X X X X X _B
00000C _H	PDRC	Port C data register	R/W	Port C	X X X X X X X X _B
00000D _H to 00000F _H	(Disabled)				
000010 _H	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0 _B
000011 _H	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0 _B
000012 _H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0 _B
000013 _H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0 _B
000014 _H	DDR4	Port 4 direction register	R/W	Port 4	0 0 0 0 0 0 0 0 _B
000015 _H	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0 _B
000016 _H	DDR6	Port 6 direction register	R/W	Port 6	0 0 0 0 0 0 0 0 _B
000017 _H	DDR7	Port 7 direction register	R/W	Port 7	— — — 0 0 0 0 0 _B
000018 _H	DDR8	Port 8 direction register	R/W	Port 8	0 0 0 0 0 0 0 0 _B
000019 _H	DDR9	Port 9 direction register	R/W	Port 9	0 0 0 0 0 0 0 0 _B
00001A _H	DDRA	Port A direction register	R/W	Port A	0 0 0 0 0 0 0 0 _B
00001B _H	DDRB	Port B direction register	R/W	Port B	0 0 0 0 0 0 0 0 _B
00001C _H	DDRC	Port C direction register	R/W	Port C	0 0 0 0 0 0 0 0 _B
00001D _H	ODR4	Port 4 output pin register	R/W	Port 4	0 0 0 0 0 0 0 0 _B
00001E _H	ADER	Analog input enable register	R/W	Port 8, 8/10-bit A/D converter	1 1 1 1 1 1 1 1 _B
00001F _H	(Disabled)				
000020 _H	SMR0	Serial mode register 0	R/W	UART0 (SCI)	0 0 0 0 0 0 0 0 _B
000021 _H	SCR0	Serial control register 0	R/W		0 0 0 0 0 1 0 0 _B

(Continued)

MB90570/A Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000022 _H	SIDR0/ SODR0	Serial input data register 0/ serial output data register 0	R/W	UART0 (SCI)	XXXXXXXX _B
000023 _H	SSR0	Serial status register 0	R/W		00001-00 _B
000024 _H	SMR1	Serial mode register 1	R/W	UART1 (SCI)	00000000 _B
000025 _H	SCR1	Serial control register 1	R/W		00000100 _B
000026 _H	SIDR1/ SODR1	Serial input data register 1/ serial output data register 1	R/W		XXXXXXXX _B
000027 _H	SSR1	Serial status register 1	R/W		00001-00 _B
000028 _H	CDCR0	Communications prescaler control register 0	R/W	Communications prescaler register 0	0---1111 _B
000029 _H	(Disabled)				
00002A _H	CDCR1	Communications prescaler control register 1	R/W	Communications prescaler register 0	0---1111 _B
00002B _H to 00002F _H	(Disabled)				
000030 _H	ENIR	DTP/interrupt enable register	R/W	DTP/external interrupt circuit	00000000 _B
000031 _H	EIRR	DTP/interrupt factor register	R/W		XXXXXXXX _B
000032 _H	ELVR	Request level setting register	R/W		00000000 _B
000033 _H					00000000 _B
000034 _H	(Disabled)				
000035 _H					
000036 _H	ADCS1	A/D control status register lower digits	R/W	8/10-bit A/D converter	00000000 _B
000037 _H	ADCS2	A/D control status register upper digits	R/W		00000000 _B
000038 _H	ADCR1	A/D data register lower digits	R		XXXXXXXX _B
000039 _H	ADCR2	A/D data register upper digits	R		00001-XX _B
00003A _H	DADR0	D/A converter data register ch.0	R/W	8-bit D/A converter	XXXXXXXX _B
00003B _H	DADR1	D/A converter data register ch.1	R/W		XXXXXXXX _B
00003C _H	DACR0	D/A control register 0	R/W		-----0 _B
00003D _H	DACR1	D/A control register 1	R/W		-----0 _B
00003E _H	CLKR	Clock output enable register	R/W	Clock monitor function	----0000 _B
00003F _H	(Disabled)				
000040 _H	PRLLO	PPG0 reload register L ch.0	R/W	8/16-bit PPG timer 0	XXXXXXXX _B
000041 _H	PRLH0	PPG0 reload register H ch.0	R/W		XXXXXXXX _B

(Continued)

MB90570/A Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000042 _H	PRL1	PPG1 reload register L ch.1	R/W	8/16-bit PPG timer 1	XXXXXXXX _B
000043 _H	PRLH1	PPG1 reload register H ch.1	R/W		XXXXXXXX _B
000044 _H	PPGC0	PPG0 operating mode control register ch.0	R/W	8/16-bit PPG timer 0	0X000XX1 _B
000045 _H	PPGC1	PPG1 operating mode control register ch.1	R/W	8/16-bit PPG timer 1	0X000001 _B
000046 _H	PPGOE	PPG0 and 1 output control registers ch.0 and ch.1	R/W	8/16-bit PPG timer 0, 1	000000XX _B
000047 _H	(Disabled)				
000048 _H	SMCSL0	Serial mode control lower status register 0	R/W	Extended I/O serial interface 0	----0000 _B
000049 _H	SMCSH0	Serial mode control upper status register 0	R/W		00000010 _B
00004A _H	SDR0	Serial data register 0	R/W		XXXXXXXX _B
00004B _H	(Disabled)				
00004C _H	SMCSL1	Serial mode control lower status register 1	R/W	Extended I/O serial interface 1	----0000 _B
00004D _H	SMCSH1	Serial mode control upper status register 1	R/W		00000010 _B
00004E _H	SDR1	Serial data register 1	R/W		XXXXXXXX _B
00004F _H	(Disabled)				
000050 _H	IPCP0	ICU data register ch.0	R	16-bit I/O timer (input capture (ICU) section)	XXXXXXXX _B
000051 _H					XXXXXXXX _B
000052 _H	IPCP1	ICU data register ch.1	R		XXXXXXXX _B
000053 _H					XXXXXXXX _B
000054 _H	ICS01	ICU control status register	R/W		00000000 _B
000055 _H	(Disabled)				
000056 _H	TCDT	Free run timer data register	R/W	16-bit I/O timer (16-bit free run timer section)	00000000 _B
000057 _H					00000000 _B
000058 _H	TCCS	Free run timer control status register	R/W		00000000 _B
000059 _H	(Disabled)				
00005A _H	OCCP0	OCU compare register ch.0	R/W	16-bit I/O timer (output compare (OCU) section)	XXXXXXXX _B
00005B _H					XXXXXXXX _B
00005C _H	OCCP1	OCU compare register ch.1	R/W		XXXXXXXX _B
00005D _H					XXXXXXXX _B
00005E _H	OCCP2	OCU compare register ch.2	R/W		XXXXXXXX _B
00005F _H					XXXXXXXX _B

(Continued)

MB90570/A Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000060 _H	OCCP3	OCU compare register ch.3	R/W	16-bit I/O timer (output compare (OCU) section)	XXXXXXXX _B
000061 _H					XXXXXXXX _B
000062 _H	OCS0	OCU control status register ch.0	R/W		0000--00 _B
000063 _H	OCS1	OCU control status register ch.1	R/W		---00000 _B
000064 _H	OCS2	OCU control status register ch.2	R/W		0000--00 _B
000065 _H	OCS3	OCU control status register ch.3	R/W		---00000 _B
000066 _H	(Disabled)				
000067 _H					
000068 _H	IBSR	I ² C bus status register	R/W	I ² C interface	00000000 _B
000069 _H	IBCR	I ² C bus control register	R/W		00000000 _B
00006A _H	ICCR	I ² C bus clock control register	R/W		--0XXXXX _B
00006B _H	IADR	I ² C bus address register	R/W		-XXXXXXXX _B
00006C _H	IDAR	I ² C bus data register	R/W		XXXXXXXX _B
00006D _H	(Disabled)				
00006E _H					
00006F _H	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	-----1 _B
000070 _H	UDCR0	Up/down count register 0	R	8/16-bit up/down counter/timer	00000000 _B
000071 _H	UDCR1	Up/down count register 1	R		00000000 _B
000072 _H	RCR0	Reload compare register 0	W		00000000 _B
000073 _H	RCR1	Reload compare register 1	W		00000000 _B
000074 _H	CSR0	Counter status register 0	R/W		00000000 _B
000075 _H	(Reserved area)* ³				
000076 _H	CCRL0	Counter control register 0	R/W	8/16-bit up/down counter/timer	-0000000 _B
000077 _H	CCRH0				00000000 _B
000078 _H	CSR1	Counter status register 1	R/W		00000000 _B
000079 _H	(Reserved area)* ³				
00007A _H	CCRL1	Counter control register 1	R/W	8/16-bit up/down counter/timer	-0000000 _B
00007B _H	CCRH1				-0000000 _B
00007C _H	SMCSL2	Serial mode control lower status register 2	R/W	Extended I/O serial interface 2	----0000 _B
00007D _H	SMCSH2	Serial mode control higher status register 2	R/W		00000010 _B
00007E _H	SDR2	Serial data register 2	R/W		XXXXXXXX _B
00007F _H	(Disabled)				

(Continued)

MB90570/A Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000080 _H	CSCR0	Chip selection control register 0	R/W	Chip select output	----0000 _B
000081 _H	CSCR1	Chip selection control register 1	R/W		----0000 _B
000082 _H	CSCR2	Chip selection control register 2	R/W		----0000 _B
000083 _H	CSCR3	Chip selection control register 3	R/W		----0000 _B
000084 _H	CSCR4	Chip selection control register 4	R/W		----0000 _B
000085 _H	CSCR5	Chip selection control register 5	R/W		----0000 _B
000086 _H	CSCR6	Chip selection control register 6	R/W		----0000 _B
000087 _H to 00008B _H	(Disabled)				
00008C _H	RDR0	Port 0 input pull-up resistor setup register	R/W	Port 0	00000000 _B
00008D _H	RDR1	Port 1 input pull-up resistor setup register	R/W	Port 1	00000000 _B
00008E _H	RDR6	Port 6 input pull-up resistor setup register	R/W	Port 6	00000000 _B
00008F _H to 00009D _H	(Disabled)				
00009E _H	PACSR	Program address detection control status register	R/W	Address match detection function	00000000 _B
00009F _H	DIRR	Delayed interrupt factor generation/cancellation register	R/W	Delayed interrupt generation module	-----0 _B
0000A0 _H	LPMCR	Low-power consumption mode control register	R/W	Low-power consumption (standby) mode	00011000 _B
0000A1 _H	CKSCR	Clock select register	R/W		11111100 _B
0000A2 _H to 0000A4 _H	(Disabled)				
0000A5 _H	ARSR	Automatic ready function select register	W	External bus pin	0011--00 _B
0000A6 _H	HACR	Upper address control register	W		00000000 _B
0000A7 _H	ECSR	Bus control signal select register	W		00000000 _B
0000A8 _H	WDTC	Watchdog timer control register	R/W	Watchdog timer	XXXXXXXX _B
0000A9 _H	TBTC	Timebase timer control register	R/W	Timebase timer	1--00100 _B
0000AA _H	WTC	Clock timer control register	R/W	Clock timer	1X000000 _B

(Continued)

MB90570/A Series

(Continued)

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
0000AB _H to 0000AD _H	(Disabled)				
0000AE _H	FMCS	Flash control register	R/W	Flash interface	0 0 0 X 0 X X 0 _B
0000AF _H	(Disabled)				
0000B0 _H	ICR00	Interrupt control register 00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
0000B1 _H	ICR01	Interrupt control register 01	R/W		0 0 0 0 0 1 1 1 _B
0000B2 _H	ICR02	Interrupt control register 02	R/W		0 0 0 0 0 1 1 1 _B
0000B3 _H	ICR03	Interrupt control register 03	R/W		0 0 0 0 0 1 1 1 _B
0000B4 _H	ICR04	Interrupt control register 04	R/W		0 0 0 0 0 1 1 1 _B
0000B5 _H	ICR05	Interrupt control register 05	R/W		0 0 0 0 0 1 1 1 _B
0000B6 _H	ICR06	Interrupt control register 06	R/W		0 0 0 0 0 1 1 1 _B
0000B7 _H	ICR07	Interrupt control register 07	R/W		0 0 0 0 0 1 1 1 _B
0000B8 _H	ICR08	Interrupt control register 08	R/W		0 0 0 0 0 1 1 1 _B
0000B9 _H	ICR09	Interrupt control register 09	R/W		0 0 0 0 0 1 1 1 _B
0000BA _H	ICR10	Interrupt control register 10	R/W		0 0 0 0 0 1 1 1 _B
0000BB _H	ICR11	Interrupt control register 11	R/W		0 0 0 0 0 1 1 1 _B
0000BC _H	ICR12	Interrupt control register 12	R/W		0 0 0 0 0 1 1 1 _B
0000BD _H	ICR13	Interrupt control register 13	R/W		0 0 0 0 0 1 1 1 _B
0000BE _H	ICR14	Interrupt control register 14	R/W		0 0 0 0 0 1 1 1 _B
0000BF _H	ICR15	Interrupt control register 15	R/W		0 0 0 0 0 1 1 1 _B
0000C0 _H to 0000FF _H	(External area)* ¹				
000100 _H to 00#### _H	(RAM area)* ²				
00#### _H to 001FEF _H	(Reserved area)* ³				
001FF0 _H	PADR0	Program address detection register 0	R/W	Program patch processing	X X X X X X X X _B
001FF1 _H		Program address detection register 1	R/W		X X X X X X X X _B
001FF2 _H		Program address detection register 2	R/W		X X X X X X X X _B
001FF3 _H	PADR1	Program address detection register 3	R/W		X X X X X X X X _B
001FF4 _H		Program address detection register 4	R/W		X X X X X X X X _B
001FF5 _H		Program address detection register 5	R/W		X X X X X X X X _B
001FF6 _H to 001FFF _H	(Reserved area)				

MB90570/A Series

Descriptions for read/write

R/W: Readable and writable

R: Read only

W: Write only

Descriptions for initial value

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

– : This bit is unused. The initial value is undefined.

*1: This area is the only external access area having an address of 0000FF_H or lower. An access operation to this area is handled as that to external I/O area.

*2: For details of the RAM area, see "■ MEMORY MAP".

*3: The reserved area is disabled because it is used in the system.

- Notes:
- For bits that is initialized by an reset operation, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.
For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.
 - The addresses following 0000FF_H are reserved. No external bus access signal is generated.
 - Boundary #####_H between the RAM area and the reserved area varies with the product model.

MB90570/A Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	EI ² OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
Reset	×	# 08	FFFFDC _H	—	—	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
INT9 instruction	×	# 09	FFFFD8 _H	—	—	
Exception	×	# 10	FFFFD4 _H	—	—	
8/10-bit A/D converter	○	# 11	FFFFD0 _H	ICR00	0000B0 _H	
Input capture 0 (ICU) include	○	# 12	FFFFCC _H			
DTP0 (external interrupt 0)	○	# 13	FFFFC8 _H	ICR01	0000B1 _H	
Input capture 1 (ICU) include	○	# 14	FFFFC4 _H			
Output compare 0 (OCU) match	○	# 15	FFFFC0 _H	ICR02	0000B2 _H	
Output compare 1 (OCU) match	○	# 16	FFFFBC _H			
Output compare 2 (OCU) match	○	# 17	FFFFB8 _H	ICR03	0000B3 _H	
Output compare 3 (OCU) match	○	# 18	FFFFB4 _H			
Extended I/O serial interface 0	○	# 19	FFFFB0 _H	ICR04	0000B4 _H	
16-bit free run timer	×	# 20	FFFFAC _H			
Extended I/O serial interface 1	○	# 21	FFFFA8 _H	ICR05	0000B5 _H	
Clock timer	×	# 22	FFFFA4 _H			
Extended I/O serial interface 2	○	# 23	FFFFA0 _H	ICR06	0000B6 _H	
DTP1 (external interrupt 1)	○	# 24	FFFF9C _H			
DTP2/DTP3 (external interrupt 2/ external interrupt 3)	○	# 25	FFFF98 _H	ICR07	0000B7 _H	
8/16-bit PPG timer 0 counter borrow	×	# 26	FFFF94 _H			
DTP4/DTP5 (external interrupt 4/ external interrupt 5)	○	# 27	FFFF90 _H	ICR08	0000B8 _H	
8/16-bit PPG timer 1 counter borrow	×	# 28	FFFF8C _H			
8/16-bit up/down counter/timer 0 borrow/overflow/inversion	○	# 29	FFFF88 _H	ICR09	0000B9 _H	
8/16-bit up/down counter/timer 0 compare match	○	# 30	FFFF84 _H			
8/16-bit up/down counter/timer 1 borrow/overflow/inversion	○	# 31	FFFF80 _H	ICR10	0000BA _H	
8/16-bit up/down counter/timer 1 compare match	○	# 32	FFFF7C _H		0000BA _H	
DTP6 (external interrupt 6)	○	# 33	FFFF78 _H	ICR11	0000BB _H	
Timebase timer	×	# 34	FFFF74 _H			

(Continued)

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(Continued)

Interrupt source	EI ² OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
DTP7 (external interrupt 7)	○	# 35	FFFF70 _H	ICR12	0000BC _H	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
I ² C interface	×	# 36	FFFF6C _H			
UART1 (SCI) reception complete	◎	# 37	FFFF68 _H	ICR13	0000BD _H	
UART1 (SCI) transmission complete	○	# 38	FFFF64 _H			
UART0 (SCI) reception complete	◎	# 39	FFFF60 _H	ICR14	0000BE _H	
UART0 (SCI) transmission complete	○	# 40	FFFF5C _H			
Flash memory	×	# 41	FFFF58 _H	ICR15	0000BF _H	
Delayed interrupt generation module	×	# 42	FFFF54 _H			

○ : Can be used

×

◎ : Can be used. With EI²OS stop function.

MB90570/A Series

■ PERIPHERALS

1. I/O Port

(1) Input/output Port

Port 0 through 4, 6, 8, A and B are general-purpose I/O ports having a combined function as an external bus pin and a resource input. Port 0 to Port 3 have a general-purpose I/O ports function only in the single-chip mode.

- Operation as output port

The pin is configured as an output port by setting the corresponding bit of the DDR register to “1”.

Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.

The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

Note: When a read-modify-write instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output, however, values of bits configured by the DDR register as inputs are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when configuring the bit used as input as outputs.

- Operation as input port

The pin is configured as an input by setting the corresponding bit of the DDR register to “0”.

When the pin is configured as an input, the output buffer is turned-off and the pin is put into a high-impedance status.

When a data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.

Reading the PDR register reads out the pin level (“0” or “1”).

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(2) Register Configuration

- Port 0 data register (PDR0)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000000 _H	(PDR1)			P07	P06	P05	P04	P03	P02	P01	P00	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 data register (PDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000001 _H	P17	P16	P15	P14	P13	P12	P11	P10	(PDR0)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 2 data register (PDR2)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000002 _H	(PDR3)			P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 data register (PDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000003 _H	P37	P36	P35	P34	P33	P32	P31	P30	(PDR2)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 4 data register (PDR4)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000004 _H	(PDR5)			P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 5 data register (PDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000005 _H	P57	P56	P55	P54	P53	P52	P51	P50	(PDR4)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 6 data register (PDR6)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000006 _H	(PDR7)			P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 data register (PDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000007 _H	—	—	—	P74	P73	P72	P71	P70	(PDR6)			— — — XXXXX _B
	—	—	—	R/W	R/W	R/W	R/W	R/W				

- Port 8 data register (PDR8)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000008 _H	(PDR9)			P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(Continued)

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- Port 9 data register (PDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000009 _H	P97	P96	P95	P94	P93	P92	P91	P90	(PDR8)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port A data register (PDRA)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00000A _H	(PDRB)			PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port B data register (PDRB)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00000B _H	(PDRA)			PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port C data register (PDRC)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00000C _H	(Disabled)			—	—	—	—	PC3	PC2	PC1	PC0	XXXXXXXX _B
				—	—	—	—	R/W	R/W	R/W	R/W	

- Port 0 direction register (DDR0)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000010 _H	(DDR1)			D07	D06	D05	D04	D03	D02	D01	D00	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 direction register (DDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000011 _H	D17	D16	D15	D14	D13	D12	D11	D10	(DDR0)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 2 direction register (DDR2)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000012 _H	(DDR3)			D27	D26	D25	D24	D23	D22	D21	D20	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 direction register (DDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000013 _H	D37	D36	D35	D34	D33	D32	D31	D30	(DDR2)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 4 direction register (DDR4)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000014 _H	(DDR5)			D47	D46	D45	D44	D43	D42	D41	D40	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

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- Port 5 direction register (DDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000015 _H	D57	D56	D55	D54	D53	D52	D51	D50	(DDR4)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 6 direction register (DDR6)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000016 _H	(DDR7)			D67	D66	D65	D64	D63	D62	D61	D60	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 direction register (DDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000017 _H	—	—	—	D74	D73	D72	D71	D70	(DDR6)			---00000 _B
	—	—	—	R/W	R/W	R/W	R/W	R/W				

- Port 8 direction register (DDR8)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000018 _H	(DDR9)			D87	D86	D85	D84	D83	D82	D81	D80	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 9 direction register (DDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000019 _H	D97	D96	D95	D94	D93	D92	D91	D90	(DDR8)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port A direction register (DDRA)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001A _H	(DDRB)			DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port B direction register (DDRB)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001B _H	(DDRA)			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port C direction register (DDRC)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001C _H	(ODR4)			—	—	—	—	DC3	DC2	DC1	DC0	00000000 _B
				—	—	—	—	R/W	R/W	R/W	R/W	

- Port 4 output pin register (ODR4)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001D _H	(DDRC)			OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 0 input pull-up resistor setup register (RDR0)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008C _H	(RDR1)			RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(Continued)

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(Continued)

- Port 1 input pull-up resistor setup register (RDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00008D _H	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	(RDR0)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- Port 6 input pull-up resistor setup register (RDR6)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008E _H	(Disabled)			RD67	RD66	RD65	RD64	RD63	RD62	RD61	RD60	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Analog input enable register (ADER)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001E _H	(Disabled)			ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable

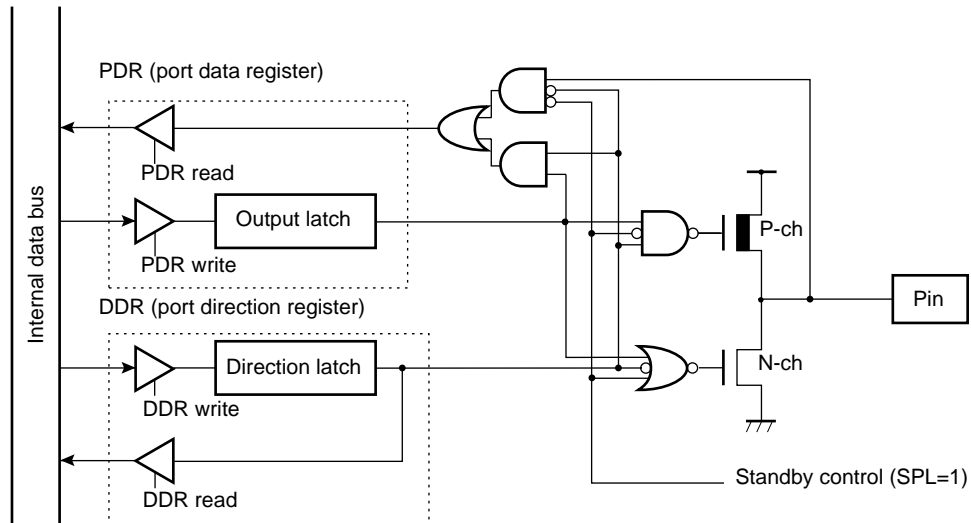
— : Reserved

X : Undefined

MB90570/A Series

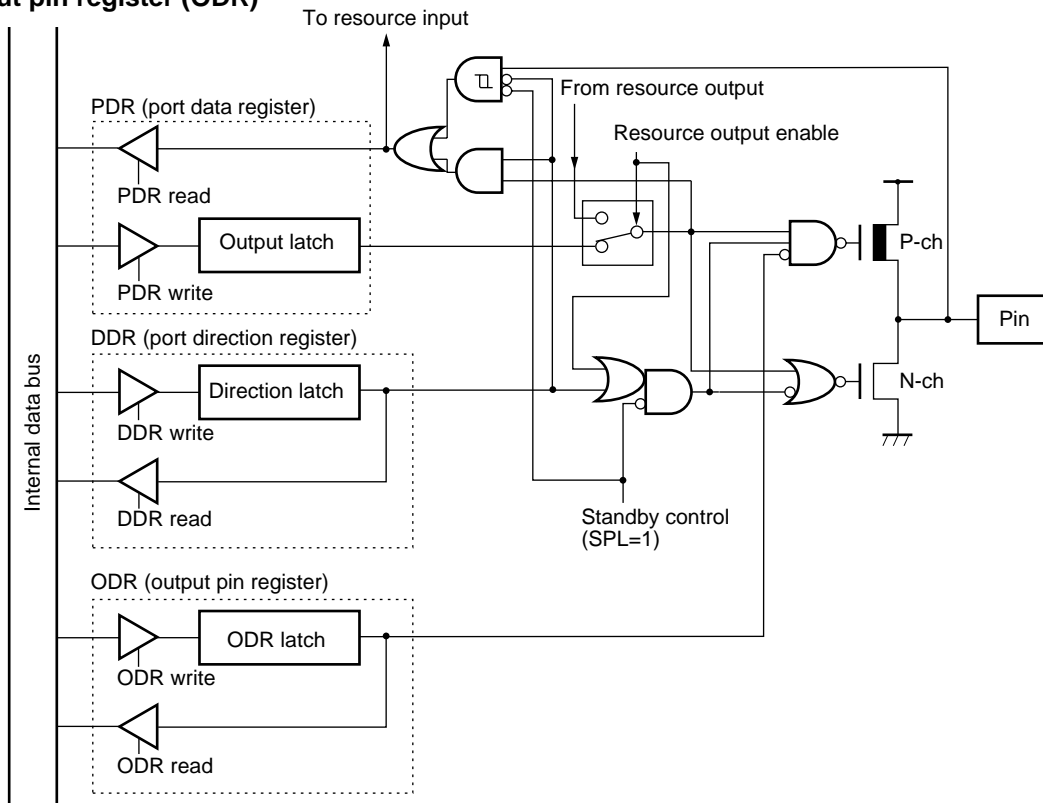
(3) Block Diagram

• Input/output port



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

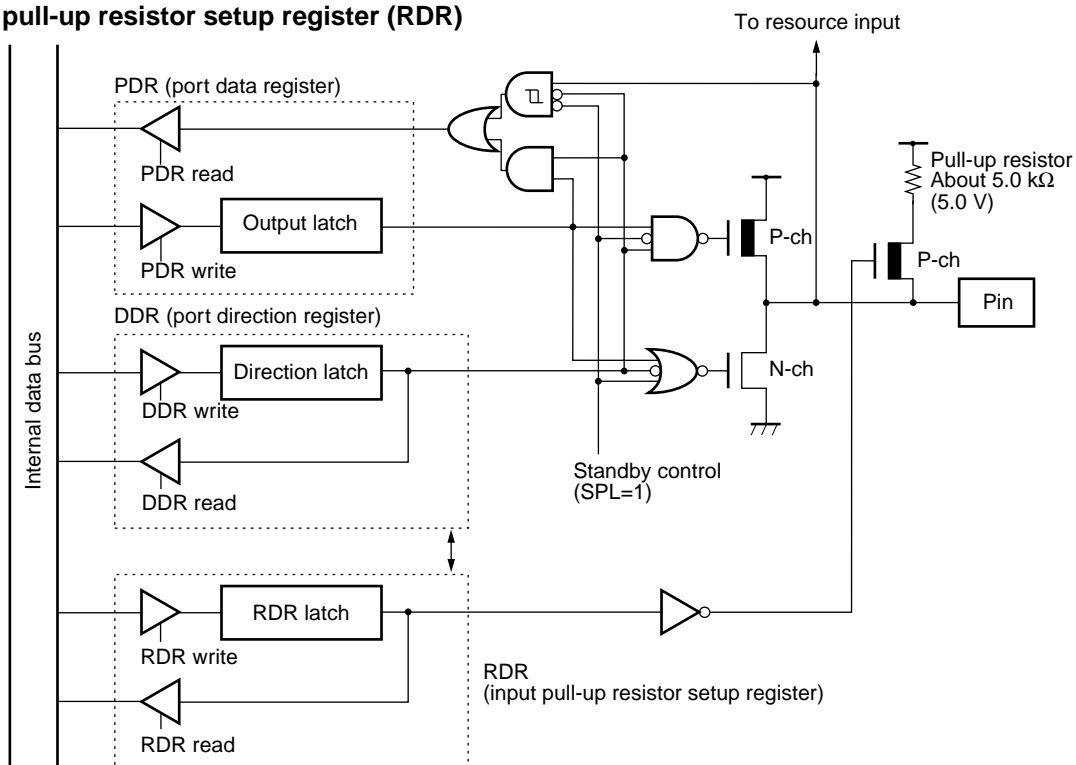
• Output pin register (ODR)



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

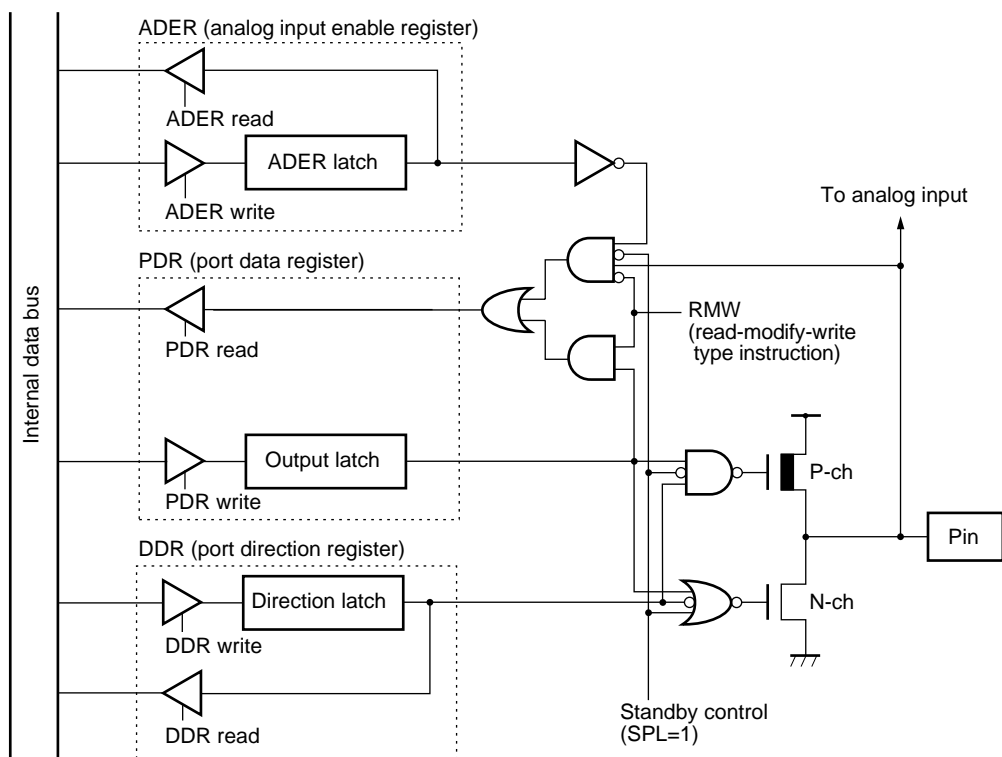
MB90570/A Series

• Input pull-up resistor setup register (RDR)



Standby control: Stop, timebase timer mode and SPL=1

• Analog input enable register (ADER)



Standby control: Stop, timebase timer mode and SPL=1

MB90570/A Series

2. Timebase Timer

The timebase timer is a 18-bit free run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types of $2^{12}/\text{HCLK}$, $2^{14}/\text{HCLK}$, $2^{16}/\text{HCLK}$, and $2^{19}/\text{HCLK}$.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer etc.

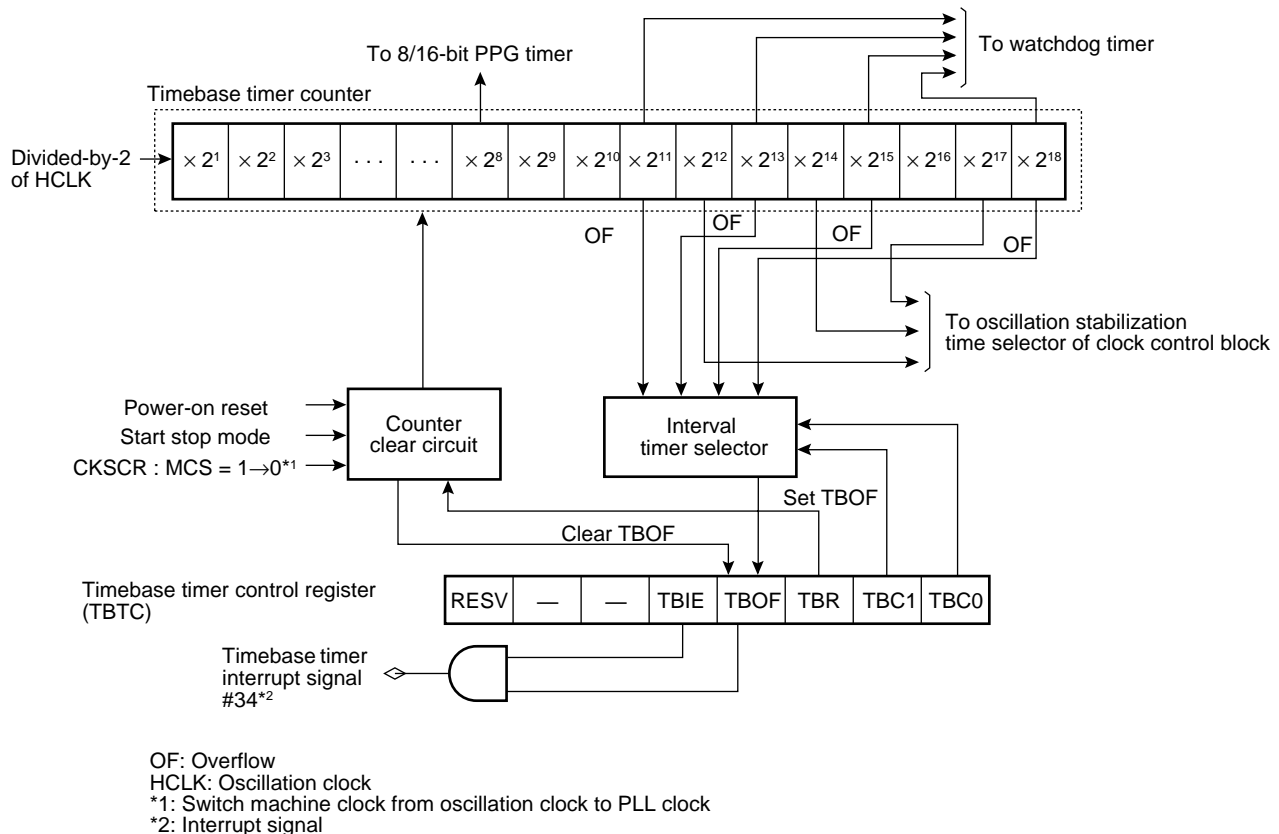
(1) Register Configuration

- Timebase timer control register (TBTC)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
0000A9 _H	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	(WDTC)			1--00100 _B
	—	—	—	R/W	R/W	W	R/W	R/W				

R/W : Readable and writable
 W : Write only
 — : Unused
 RESV : Reserved bit

(2) Block Diagram



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3. Watchdog Timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

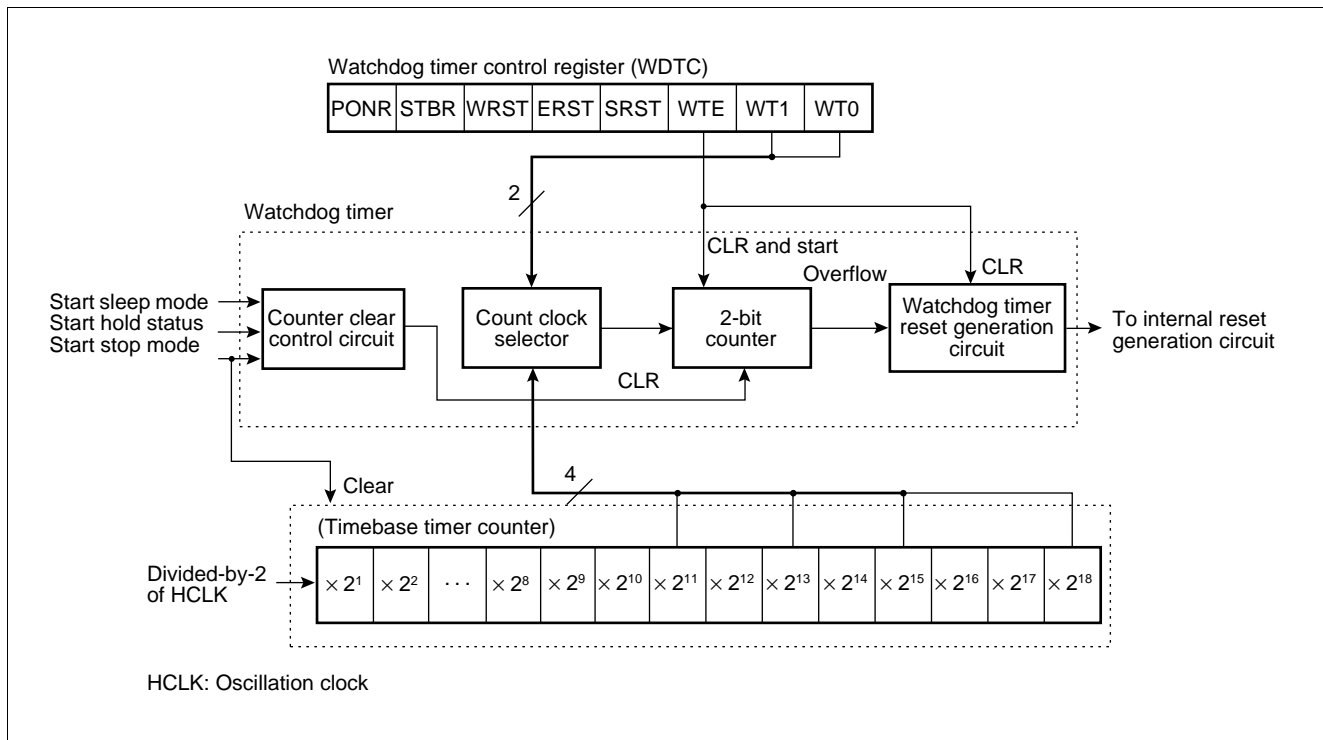
(1) Register Configuration

- Watchdog timer control register (WDTC)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A8 _H	(TBTC)			PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXXXXX _B
				R	R	R	R	R	W	W	W	

R : Read only
 W : Write only
 X : Indeterminate

(2) Block Diagram



MB90570/A Series

4. 8/16-bit PPG Timer

The 8/16-bit PPG timer is a 2-CH reload timer module for outputting pulse having given frequencies/duty ratios.

The two modules performs the following operation by combining functions.

- 8-bit PPG output 2-CH independent operation mode
This is a mode for operating independent 2-CH 8-bit PPG timer, in which PPG0 and PPG1 pins correspond to outputs from PPG0 and PPG1 respectively.
- 16-bit PPG timer output operation mode
In this mode, PPG0 and PPG1 are combined to be operated as a 1-CH 8/16-bit PPG timer operating as a 16-bit timer. Because PPG0 and PPG1 outputs are reversed by an underflow from PPG1 outputting the same output pulses from PPG0 and PPG1 pins.
- 8 + 8-bit PPG timer output operation mode
In this mode, PPG0 is operated as an 8-bit communications prescaler, in which an underflow output of PPG0 is used as a clock source for PPG1. A toggle output of PPG0 and PPG output of PPG1 are output from PPG0 and PPG1 respectively.
- PPG output operation
A pulse wave with any period/duty ratio is output. The module can also be used as a D/A converter with an external add-on circuit.

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(1) Register Configuration

- PPG0 operating mode control register ch.0 (PPGC0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000044 _H	(PPGC1)							PEN0	—	PE00	PIE0	PUF0	—	—	—	RESV	0X000XX1 _B
								R/W		R/W	R/W	R/W					

- PPG1 operating mode control register ch.1 (PPGC1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000045 _H	PEN1	—	PEI0	PIE1	PUF1	MD1	MD0	RESV	(PPGC0)								0X000001 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

- PPG0, 1 output control register ch.0 (PPGOE)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000046 _H	(Disabled)							PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	—	—	—	000000XX _B
								R/W	R/W	R/W	R/W	R/W	R/W				

- PPG0 reload register H ch.0 (PRLH0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000041 _H																(PRL0)	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								

- PPG1 reload register H ch.1 (PRLH1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000043 _H																(PRL1)	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								

- PPG0 reload register L ch.0 (PRL0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000040 _H	(PRL0)																XXXXXXXX _B
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 reload register L ch.1 (PRL1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000042 _H	(PRL1)																XXXXXXXX _B
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable

— : Reserved

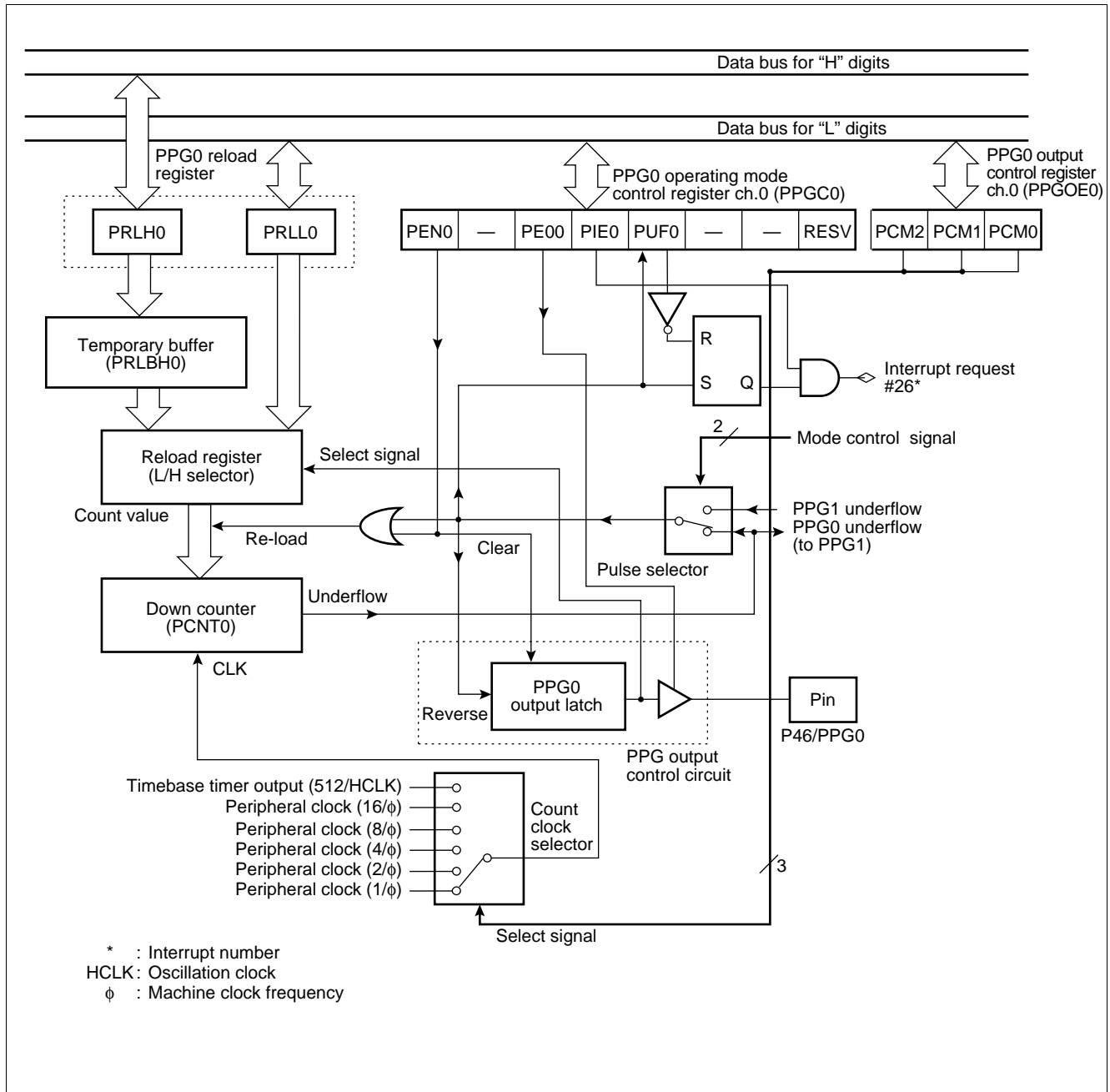
X : Undefined

RESV : Reserved bit

MB90570/A Series

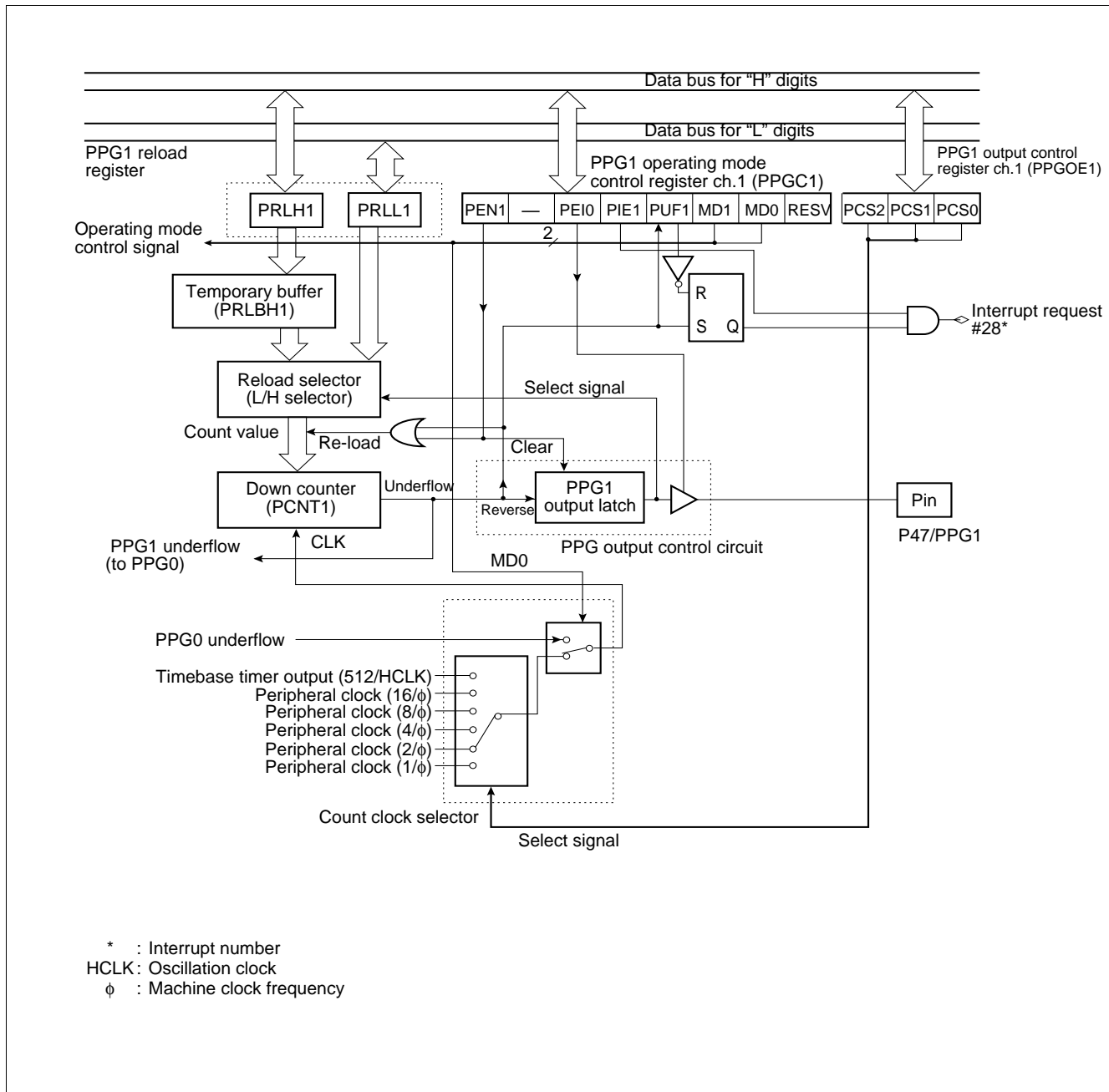
(2) Block Diagram

• Block diagram of 8/16-bit PPG timer (ch.0)



MB90570/A Series

• Block diagram of 8/16-bit PPG timer (ch.1)

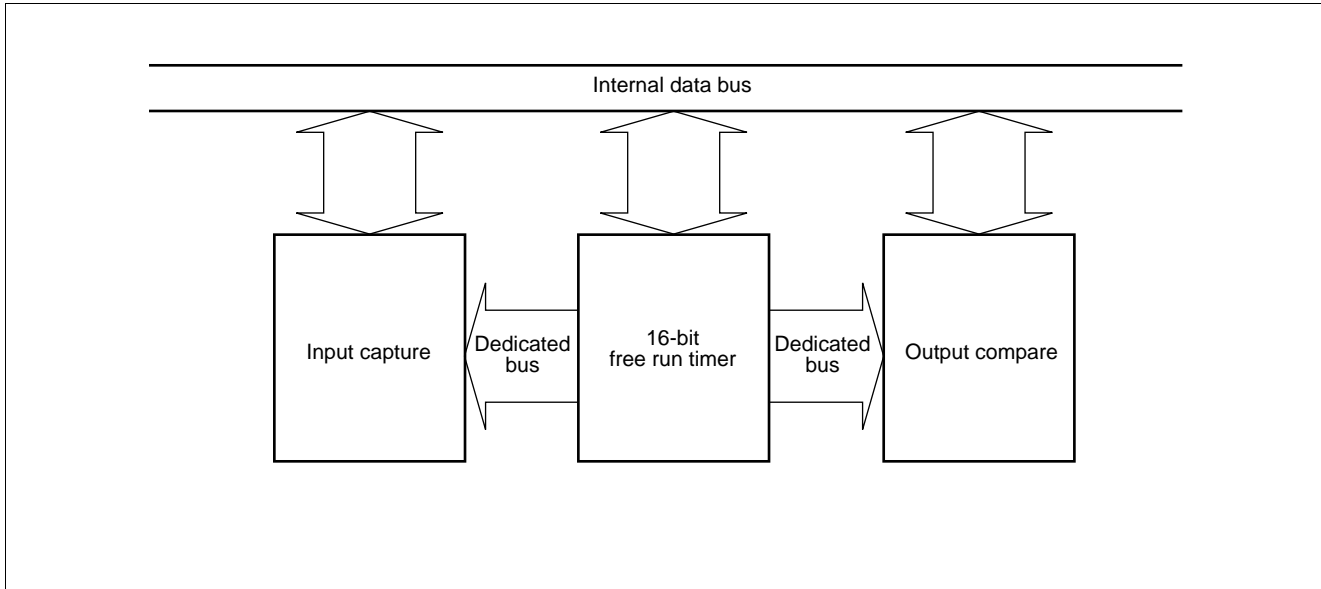


MB90570/A Series

5. 16-bit I/O timer

The 16-bit I/O timer module consists of one 16-bit free run timer, two input capture circuits, and four output comparators. This module allows two independent waveforms to be output on the basis of the 16-bit free run timer. Input pulse width and external clock periods can, therefore, be measured.

- **Block Diagram**



MB90570/A Series

(1) 16-bit free run Timer

The 16-bit free run timer consists of a 16-bit up counter, a control register, and a communications prescaler register. The value output from the timer counter is used as basic timer (base timer) for input capture (ICU) and output compare (OCU).

- A counter operation clock can be selected from four internal clocks ($\phi/4$, $\phi/16$, $\phi/32$ and $\phi/64$).
- An interrupt can be generated by overflow of counter value or compare match with OCU compare register 0. (Compare match requires mode setup.)
- The counter value can be initialized to "0000_H" by a reset, software clear or compare match with OCU compare register 0.

• Register Configuration

- free run timer data register (TCDT)

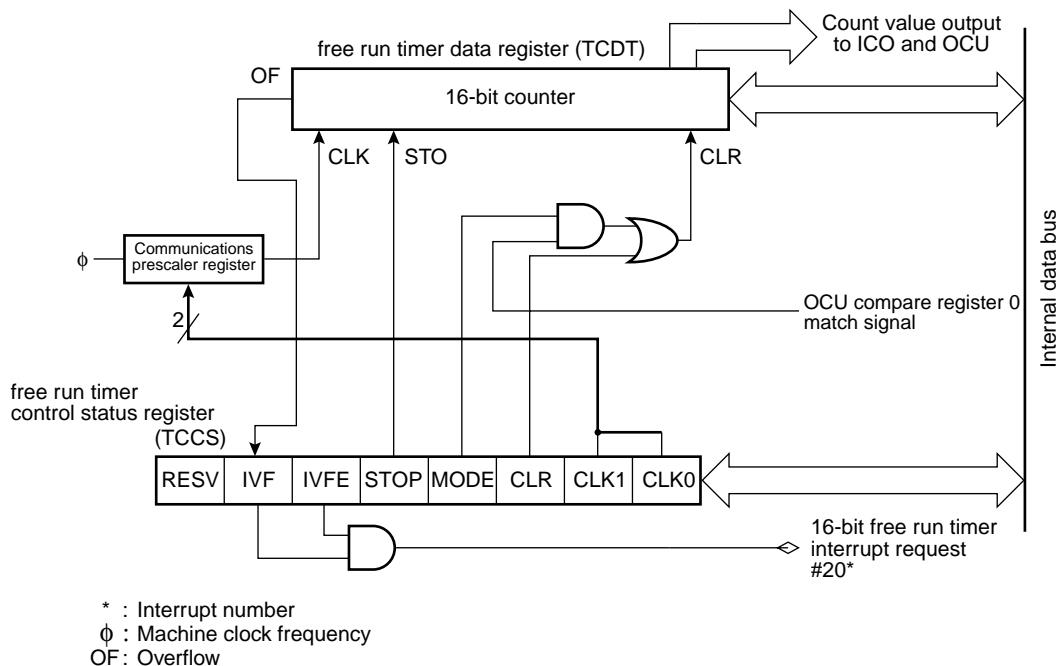
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000056 _H 000057 _H	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- free run timer control status register (TCCS)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000058 _H	(Disabled)								RESV	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0	00000000 _B
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
RESV : Reserved bit

• Block Diagram



MB90570/A Series

(2) Input Capture (ICU)

The input capture (ICU) generates an interrupt request to the CPU simultaneously with a storing operation of current counter value of the 16-bit free run timer to the ICU data register (IPCP) upon an input of a trigger edge to the external pin.

There are four sets (four channels) of the input capture external pins and ICU data registers, enabling measurements of maximum of four events.

- The input capture has two sets of external input pins (IN0, IN1) and ICU registers (IPCP), enabling measurements of maximum of four events.
- A trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 16-bit free run timer to the ICU data register (IPCP).
- The input compare conforms to the extended intelligent I/O service (EI²OS).
- The input capture (ICU) function is suited for measurements of intervals (frequencies) and pulse widths.

• Register Configuration

• ICU data register ch.0, ch.1 (IPCP0, IPCP1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
IPCP0(high): 000051 _H IPCP1(high): 000053 _H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	(IPCP0 low, IPCP1 low)			XXXXXXXX _B
	R	R	R	R	R	R	R	R				
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
IPCP0(low): 000050 _H IPCP1(low): 000052 _H	(IPCP0 high, IPCP1 high)			CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXX _B
				R	R	R	R	R	R	R	R	

Note: This register holds a 16-bit free run timer value when the valid edge of the corresponding external pin input waveform is detected. (You can word-access this register, but you cannot program it.)

• ICU control status register (ICS01)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000054 _H	(Disabled)			ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

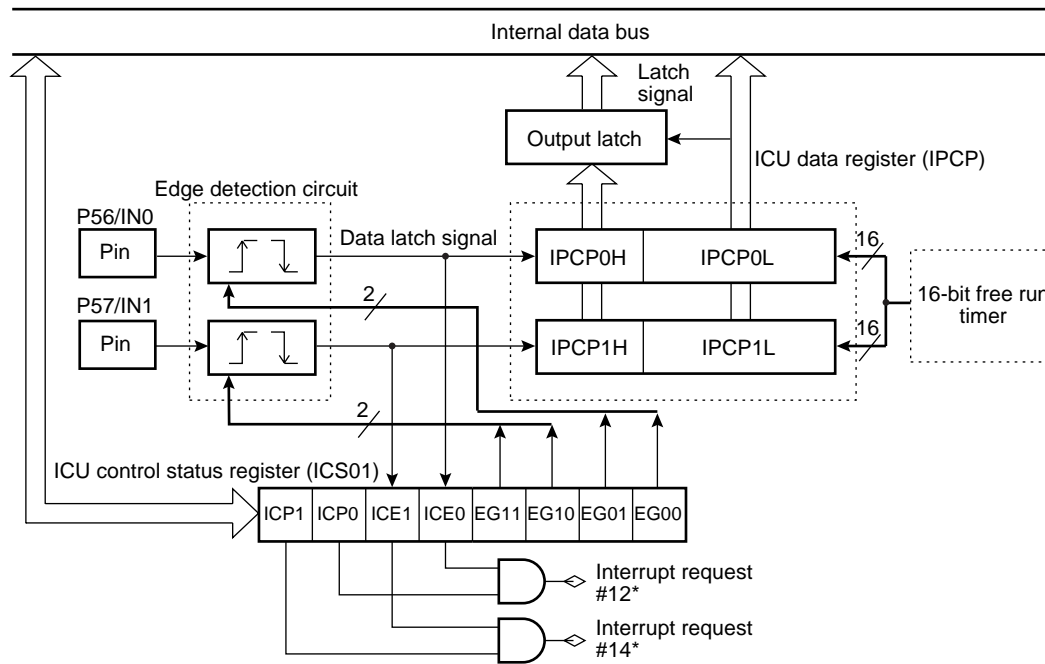
R/W : Readable and writable

R : Read only

X : Undefined

MB90570/A Series

• Block Diagram



* : Interrupt number

MB90570/A Series

(3) Output Compare (OCU)

The output compare (OCU) is two sets of compare units consisting of four-channel OCU compare registers, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 16-bit free run timer.

The OUT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the CMOD bit.

• Register Configuration

• OCU control status register ch.1, ch.3 (OCS1, OCS3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....bit 0	Initial value
000063 _H 000065 _H	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	(OCS0, OCS2)	---00000 _B
	—	—	—	R/W	R/W	R/W	R/W	R/W		

• OCU control status register ch.0, ch.2 (OCS0, OCS2)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000062 _H 000064 _H	(OCS1, OCS3)	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000 - 00 _B
		R/W	R/W	R/W	R/W	—	—	R/W	R/W	

• OCU compare register ch.0 to ch.3 (OCCP0 to OCCP3)

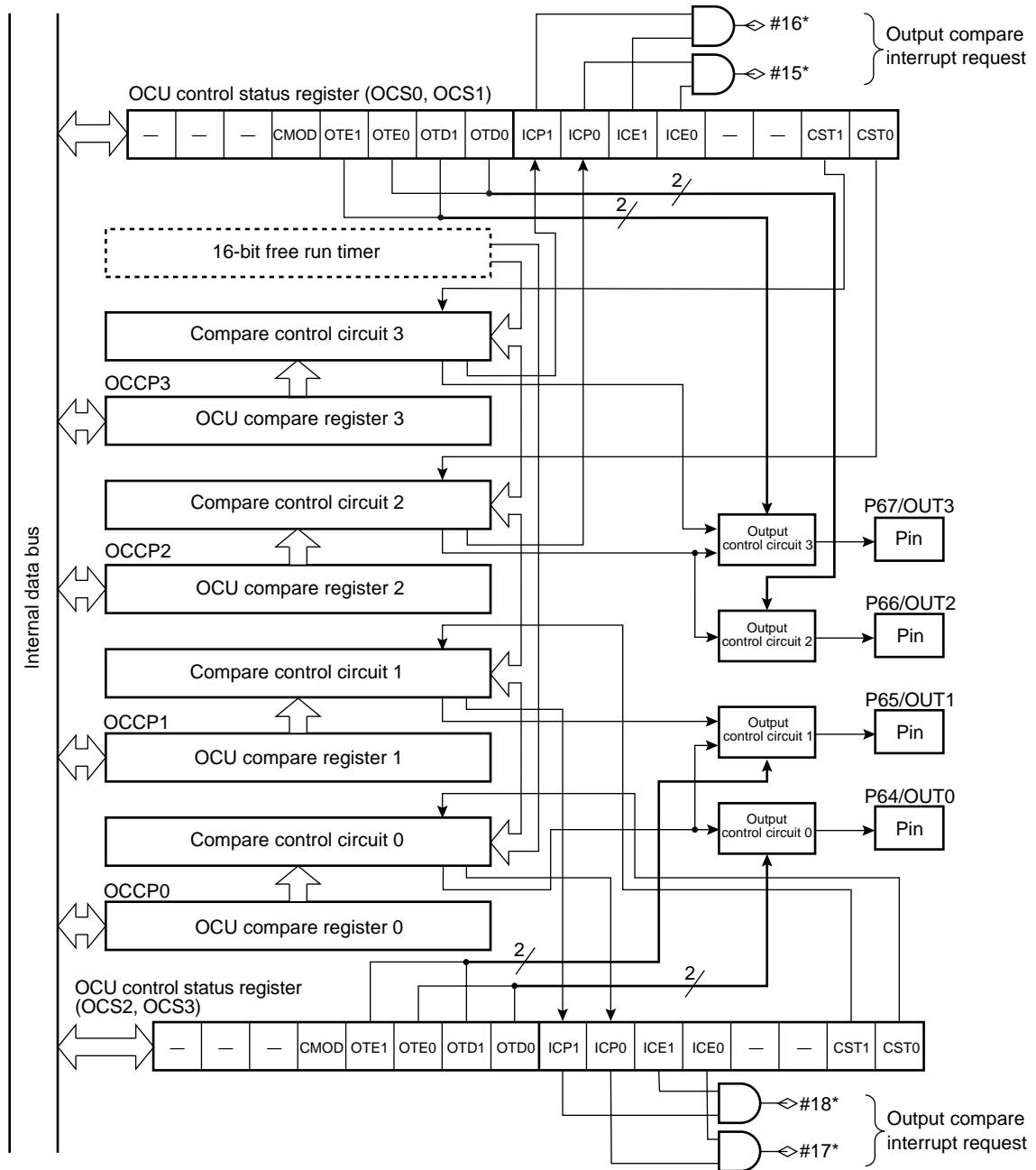
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
OCCP0 (high order address) : 00005B _H OCCP1 (high order address) : 00005D _H OCCP2 (high order address) : 00005F _H OCCP3 (high order address) : 000061 _H	C15	C14	C13	C12	C11	C10	C09	C08	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
OCCP0 (low order address) : 00005A _H OCCP1 (low order address) : 00005C _H OCCP2 (low order address) : 00005E _H OCCP3 (low order address) : 000060 _H	C07	C06	C05	C04	C03	C02	C01	C00	XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Reserved
X : Undefined

MB90570/A Series

• Block diagram



* : Interrupt number

MB90570/A Series

6. 8/16-bit up/down counter/timer

The 8/16-bit up/down counter/timer consists of six event input pins, two 8-bit up/down counters, two 8-bit reload compare registers, and their controllers.

(1) Register configuration

• Up/down count register 0 (UDCR0)										
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	Initial value
000070 _H	(UDCR1)							D07	D06	00000000 _B
								R	R	
								R	R	
								R	R	
								R	R	
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								R	R	

R/W : Readable and writable

R : Read only

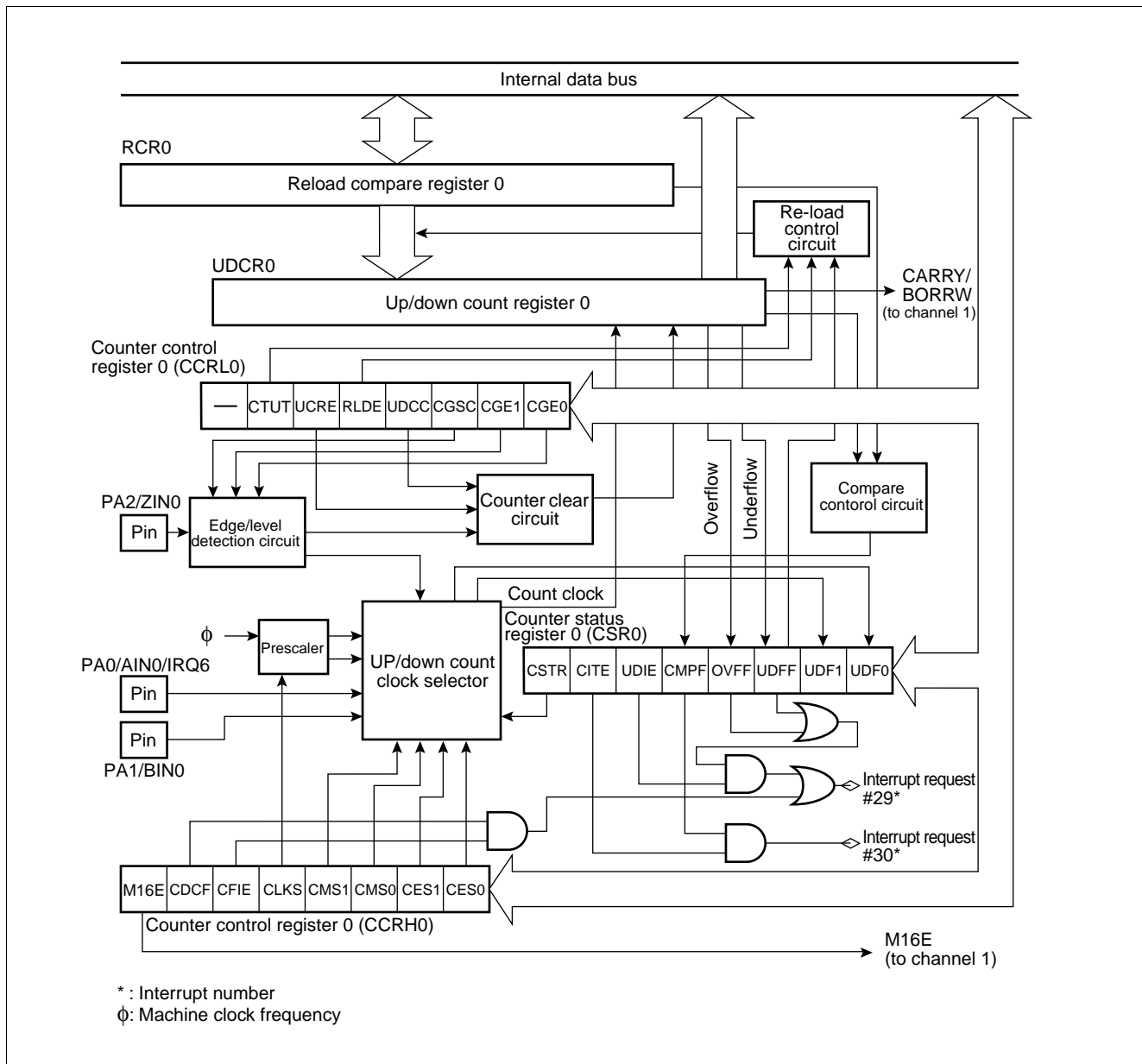
W : Write only

— : Undefined

MB90570/A Series

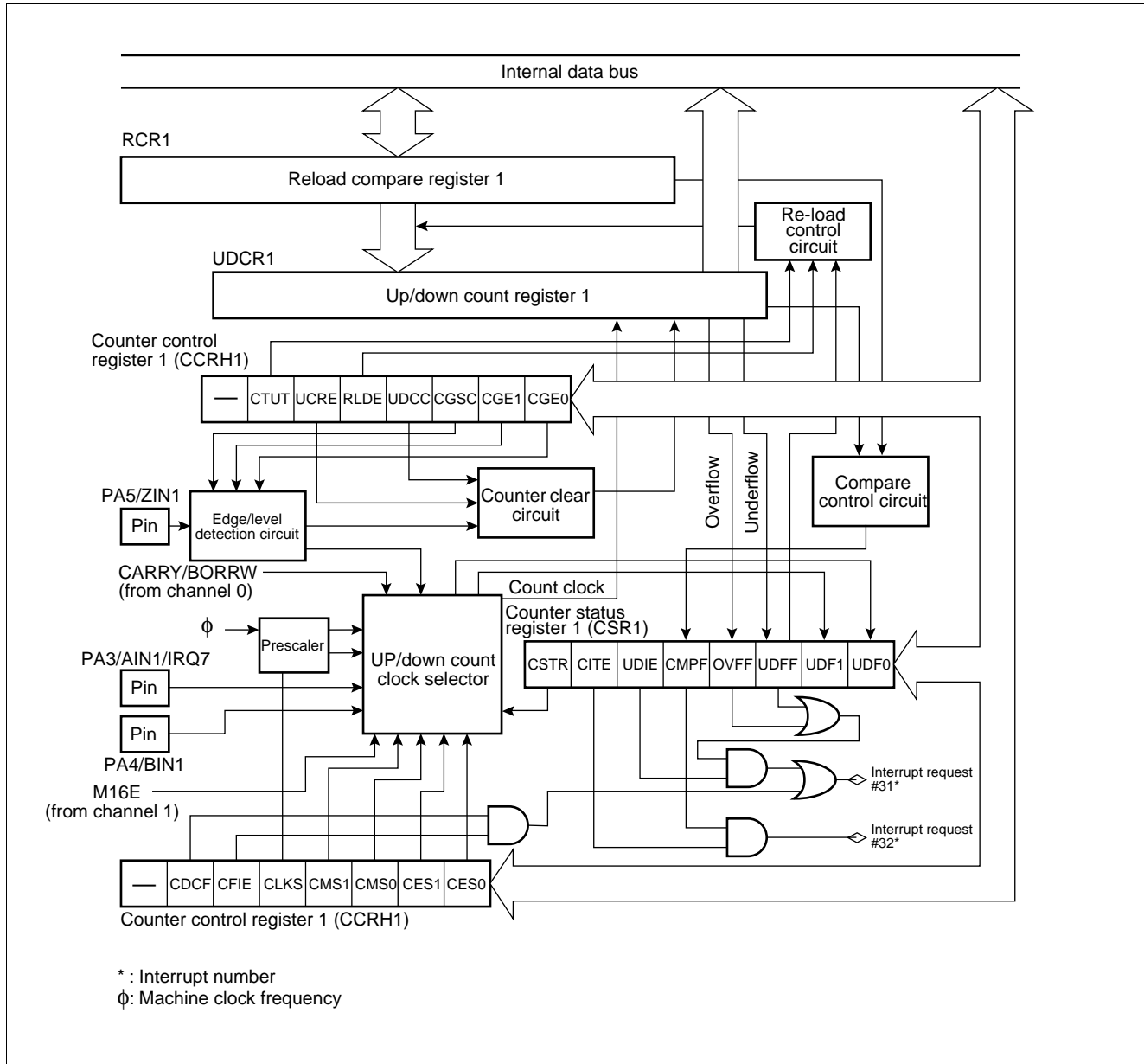
(2) Block Diagram

• Block diagram of 8/16-bit up/down counter/timer 0



MB90570/A Series

• Block diagram of 8/16-bit up/down counter/timer 1



MB90570/A Series

7. Extended I/O serial interface

The extended I/O serial interface transfers data using a clock synchronization system having an 8-bit x 1 channel configuration.

For data transfer, you can select LSB first/MSB first.

(1) Register Configuration

- Serial mode control upper status register 0 to 2 (SMCSH0 to SMCSH2)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7..... bit 0	Initial value
SMCSH0 : 000049 _H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	(SMCSL)	00000010 _B
SMCSH1 : 00004D _H										
SMCSH2 : 00007D _H										
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W		

- Serial mode control lower status register 0 to 2 (SMCSL0 to SMCSL2)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SMCSL0 : 000048 _H	(SMCSH)			—	—	—	—	MODE	BDS	SOE	SCOE	- - - - 0000 _B
SMCSL1 : 00004C _H												
SMCSL2 : 00007C _H												
				—	—	—	—	R/W	R/W	R/W	R/W	

- Serial data register 0 to 2 (SDR0 to SDR2)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SDR0 : 00004A _H	(Disabled)			D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
SDR1 : 00004E _H												
SDR2 : 00007E _H												
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable

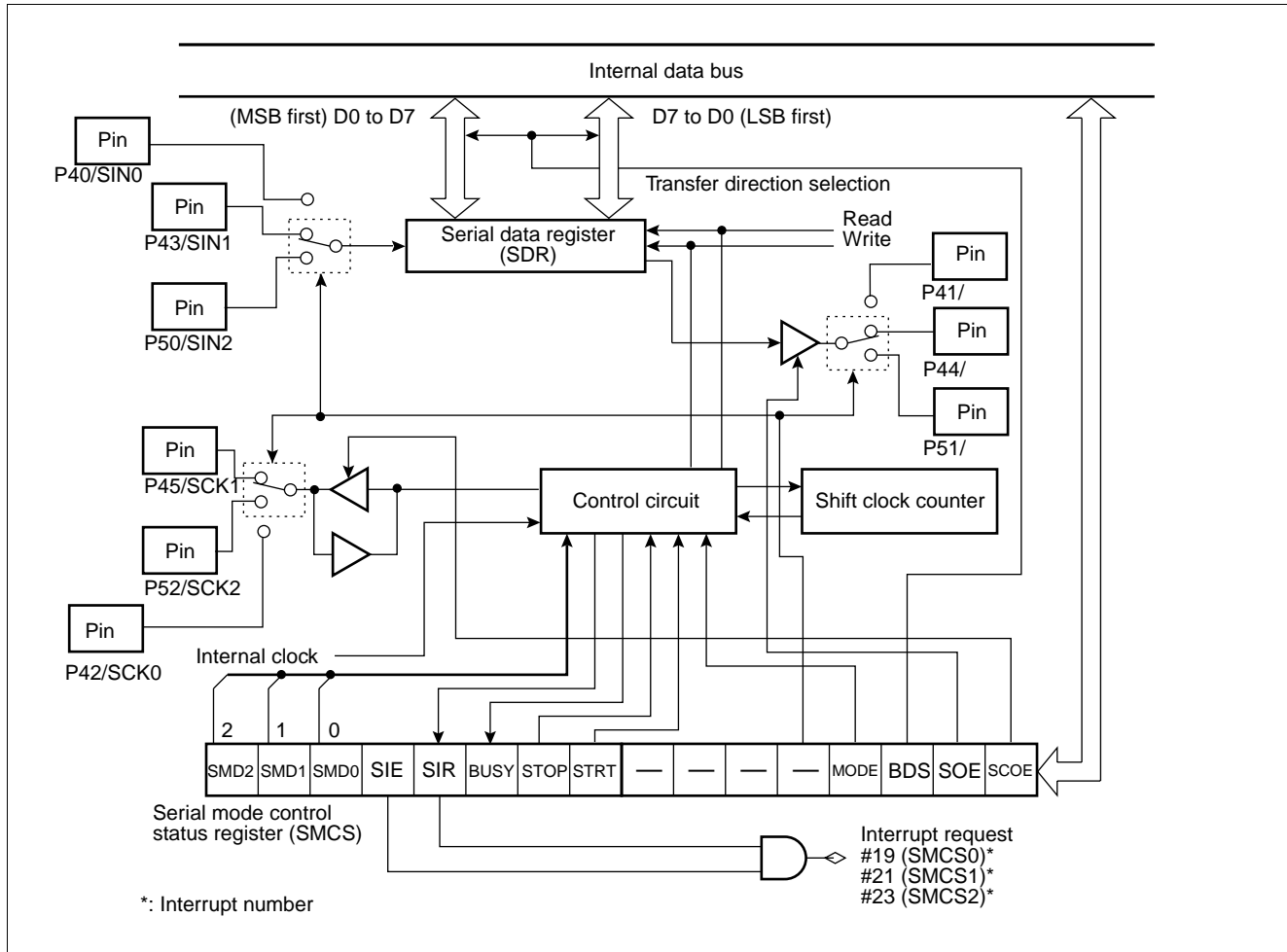
R : Read only

— : Reserved

X : Undefined

MB90570/A Series

(2) Block Diagram



MB90570/A Series

8. I²C Interface

The I²C interface is a serial I/O port supporting Inter IC BUS operating as master/slave devices on I²C bus.

The MB90570/A series contains one channel of an I²C interface, having the following features.

- Master/slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transmission direction detection function
- Repeated generation function start condition and detection function
- Bus error detection function

(1) Register Configuration

• I²C bus status register (IBSR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000068 _H	(IBCR)								BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	00000000 _B
									R	R	R	R	R	R	R	R	

• I²C bus control register (IBCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000069 _H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	(IBSR)								00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

• I²C bus clock control register (ICCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00006A _H	(IADR)								—	—	EN	CS4	CS3	CS2	CS1	CS0	--0XXXXX _B
									—	—	R/W	R/W	R/W	R/W	R/W	R/W	

• I²C bus address register (IADR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00006B _H	—	A6	A5	A4	A3	A2	A1	A0	(ICCR)								-XXXXXXXX _B
	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

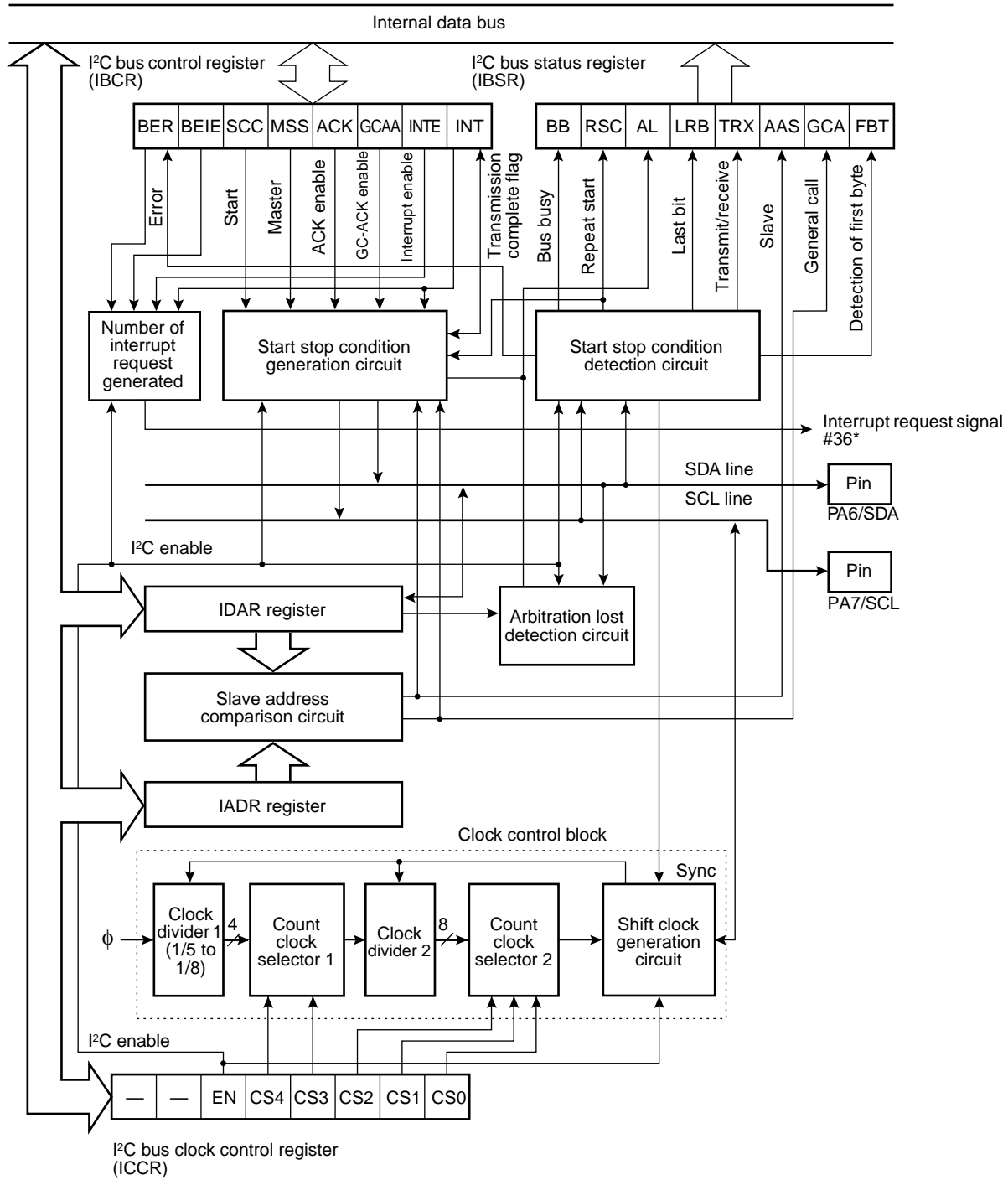
• I²C bus data register (IDAR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00006C _H	(Disabled)								D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
 R : Read only
 — : Reserved
 X : Indeterminate

MB90570/A Series

(2) Block Diagram



ϕ : Machine clock frequency
 *: Interrupt number

MB90570/A Series

9. UART0 (SCI), UART1 (SCI)

UART0 (SCI) and UART1 (SCI) are general-purpose serial data communication interfaces for performing synchronous or asynchronous communication (start-stop synchronization system).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
Clock asynchronous (start-stop synchronization system)
- Baud rate: Embedded dedicated baud rate generator
External clock input possible
Internal clock (a clock supplied from 16-bit reload timer 0 can be used.)

Asynchronization 9615 bps/31250 bps/4808 bps/2404 bps/1202 bps CLK synchronization 1 Mbps/500 kbps/250 kbps/125 kbps/62.5 kbps	}	Internal machine clock For 6 MHz, 8 MHz, 10 MHz, 12 MHz and 16 MHz
---	---	--
- Data length: 7 bit to 9 bit selective (without a parity bit)
6 bit to 8 bit selective (with a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
Overrun error
Parity error (multi-processor mode is supported, enabling setup of any baud rate by an external clock.)
- Interrupt request: Receive interrupt (receive complete, receive error detection)
Transmit interrupt (transmission complete)
Transmit/receive conforms to extended intelligent I/O service (EI²OS)

MB90570/A Series

(1) Register Configuration

- Serial control register 0,1 (SCR0, SCR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....bit 0	Initial value
000021 _H 000025 _H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	(SMR0, SMR1)	00000100 _B
	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W		

- Serial mode register 0, 1 (SMR0, SMR1)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000020 _H 000024 _H	(SCR0, SCR1)	MD1	MD0	CS2	CS1	CS0	RESV	SCKE	SOE	00000000 _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Serial status register 0,1 (SSR0, SSR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....bit 0	Initial value
000023 _H 000027 _H	PE	ORE	FRE	RDRF	TRDE	—	RIE	TIE	(SIDR0, SIDR1/SODR0,SODR1)	00001-00 _B
	R	R	R	R	R	—	R/W	R/W		

- Serial input data register 0,1 (SIDR0, SIDR1)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H 000026 _H	(SSR0, SSR1)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
		R	R	R	R	R	R	R	R	

- Serial output data register 0,1 (SODR0, SODR1)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H 000026 _H	(SSR0, SSR1)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
		W	W	W	W	W	W	W	W	

- Communications prescaler control register 0,1 (CDCR0, CDCR1)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000028 _H 00002A _H	(Disabled)	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0---1111 _B
		R/W	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable

R : Read only

W : Write only

— : Reserved

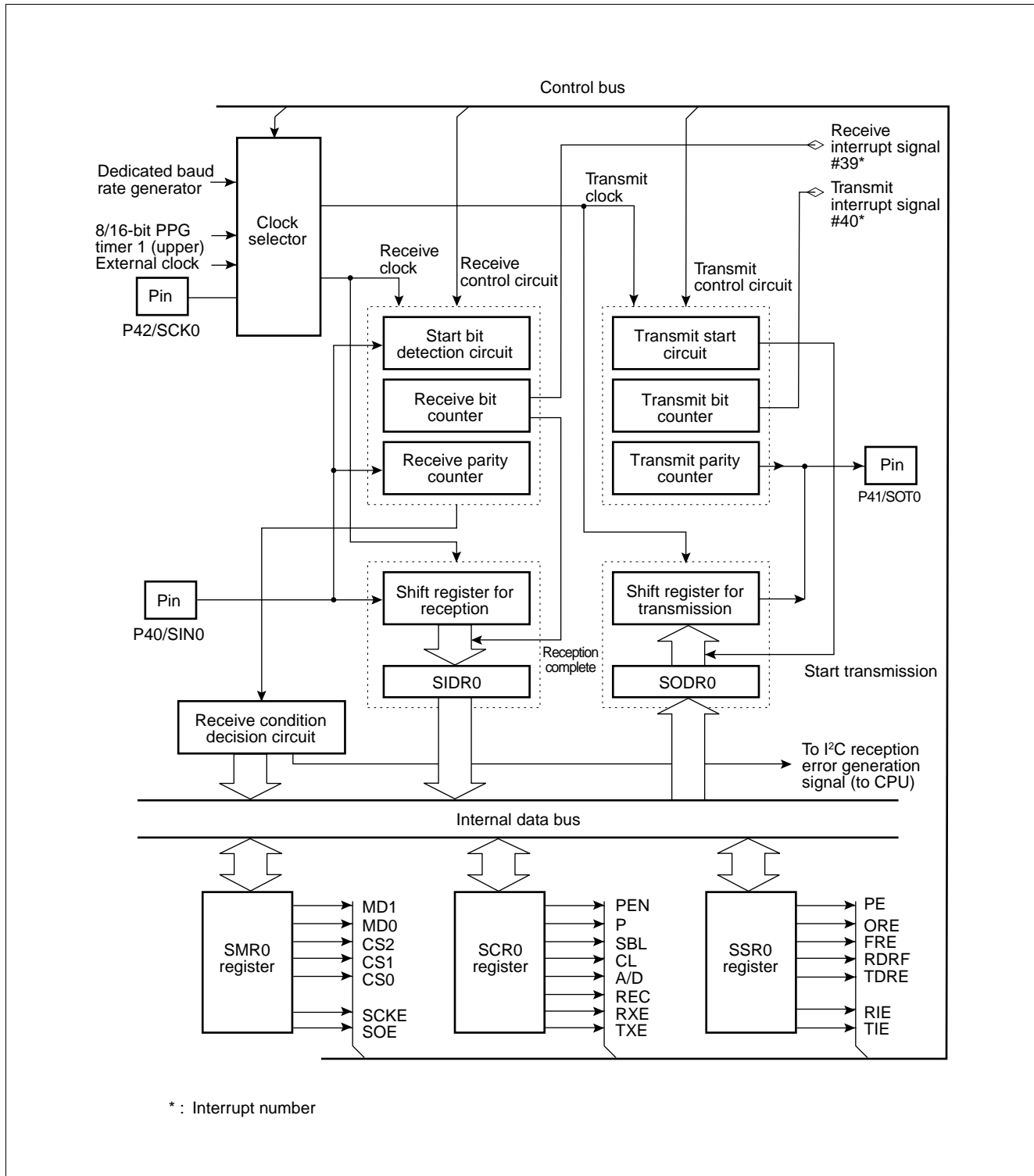
X : Undefined

RESV : Reserved bit

MB90570/A Series

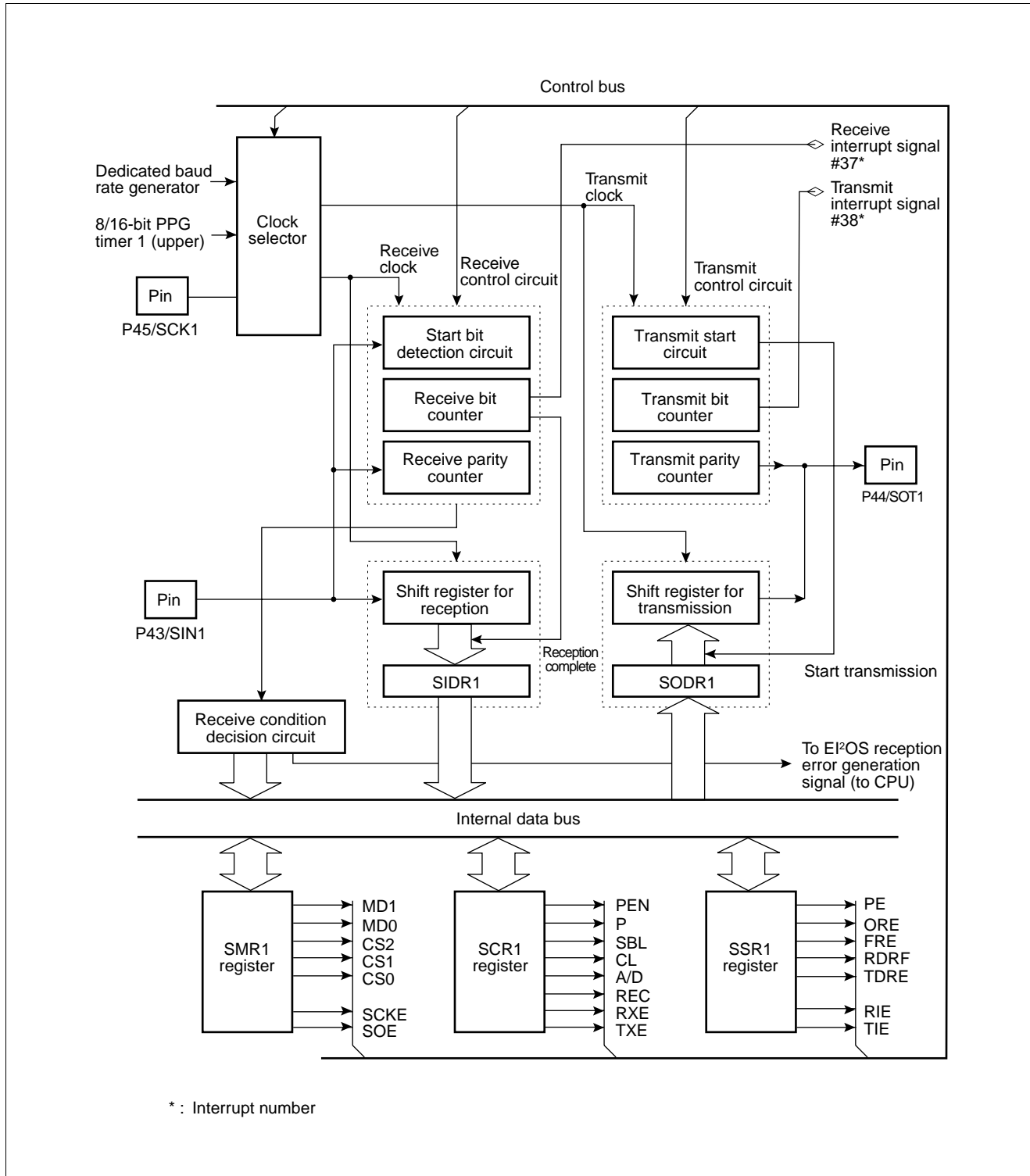
(2) Block Diagram

• UART0 (SCI)



MB90570/A Series

• UART1 (SCI)



MB90570/A Series

10. DTP/External Interrupt Circuit

DTP (Data Transfer Peripheral), which is located between the peripheral circuit outside the device and the F²MC-16LX CPU, receives an interrupt request or DMA request generated by the external peripheral circuit* for transmission to the F²MC-16LX CPU. DTP is used to activate the intelligent I/O service or interrupt processing. As request levels for IRQ2 to IRQ7, two types of “H” and “L” can be selected for the intelligent I/O service. Rising and falling edges as well as “H” and “L” can be selected for an external interrupt request. For IRQ0 and IRQ1, a request by a level cannot be entered, but both edges can be entered.

* : The external peripheral circuit is connected outside the MB90570/A series device.

Note: IRQ0 and IRQ1 cannot be used for the intelligent I/O service and return from an interrupt.

(1) Register Configuration

- DTP/interrupt factor register (EIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000031 _H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	(ENIR)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- DTP/interrupt enable register (ENIR)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000030 _H	(EIRR)			EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Request level setting register (ELVR)

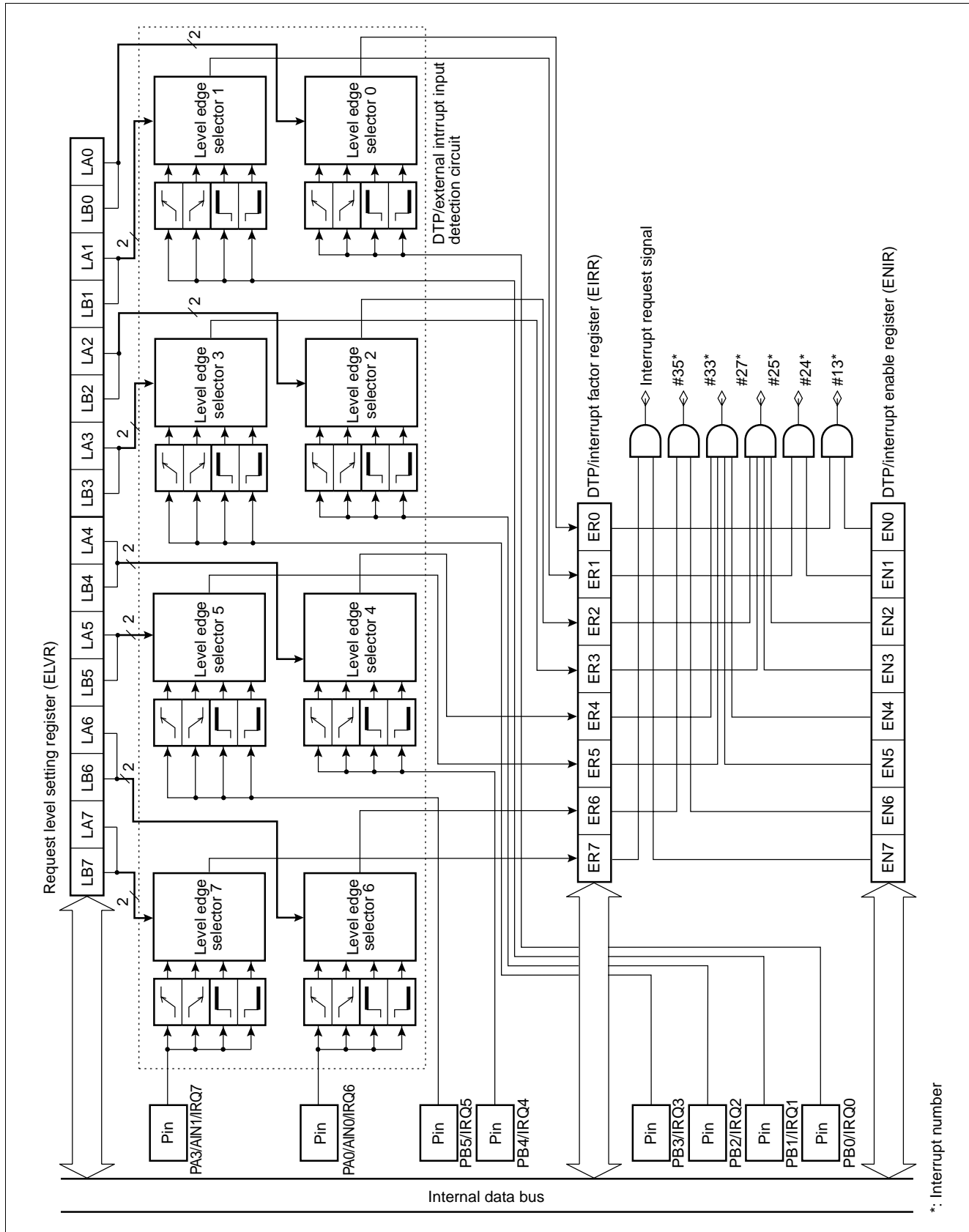
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
Low order address 000032 _H	(ELVR upper)			LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
High order address 000033 _H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	(ELVR lower)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

R/W: Readable and writable
X : Undefined

MB90570/A Series

(2) Block Diagram



MB90570/A Series

11. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks for development on a real-time operating system (REALOS series). The module can be used to generate softwarewise generates hardware interrupt requests to the CPU and cancel the interrupts.

This module does not conform to the extended intelligent I/O service (EI²OS).

(1) Register Configuration

• Delayed interrupt factor generation/cancellation register (DIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00009F _H	—	—	—	—	—	—	—	R0			(PACSR)	-----0 _B
	—	—	—	—	—	—	—	R/W				

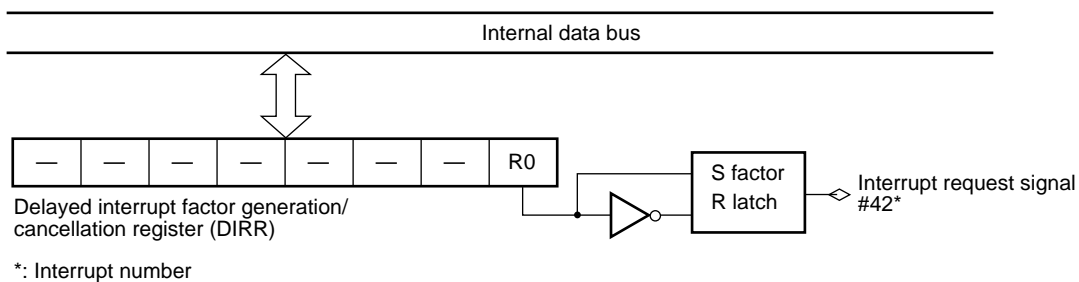
Note: Upon a reset, an interrupt is canceled.

R/W: Readable and writable

— : Reserved

The DIRR is the register used to control delay interrupt request generation/cancellation. Programming this register with “1” generates a delay interrupt request. Programming this register with “0” cancels a delay interrupt request. Upon a reset, an interrupt is canceled. The reserved bit area can be programmed with either “0” or “1”. For future extension, however, it is recommended that bit set and clear instructions be used to access this register.

(2) Block Diagram



MB90570/A Series

12. 8/10-bit A/D Converter

The 8/10-bit A/D converter has a function of converting analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features.

- Minimum conversion time: 26.3 μ s (at machine clock of 16 MHz, including sampling time)
- Minimum sampling time: 4 μ s/256 μ s (at machine clock of 16 MHz)
- Compare time: 176/352 machine cycles per channel (176 machine cycles are used for a machine clock below 8 MHz.)
- Conversion method: RC successive approximation method with a sample and hold circuit.
- 8-bit or 10-bit resolution
- Analog input pins: Selectable from eight channels by software
 - Single conversion mode: Selects and converts one channel.
 - Scan conversion mode: Converts two or more successive channels. Up to eight channels can be programmed.
 - Continuous conversion mode: Repeatedly converts specified channels.
 - Stop conversion mode: Stops conversion after completing a conversion for one channel and wait for the next activation (conversion can be started synchronously.)
- Interrupt requests can be generated and the extended intelligent I/O service (EI²OS) can be started after the end of A/D conversion. Furthermore, A/D conversion result data can be transferred to the memory, enabling efficient continuous processing.
- When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
- Starting factors for conversion: Selected from software activation, and external trigger (falling edge).

MB90570/A Series

(1) Register Configuration

- A/D control status register upper digits (ADCS2)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000037 _H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	RESV	(ADCS1)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- A/D control status register lower digits (ADCS1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000036 _H	(ADCS2)			MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- A/D data register upper digits (ADCR2)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000039 _H	DSEL	ST1	ST0	CT1	XCT0	—	D9	D8	(ADCR1)			00001-XX _B
	W	W	W	W	W	—	—	—				

- A/D data register lower digits (ADCR1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000038 _H	(ADCR2)			D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
				R	R	R	R	R	R	R	R	

R/W: Readable and writable

R : Read only

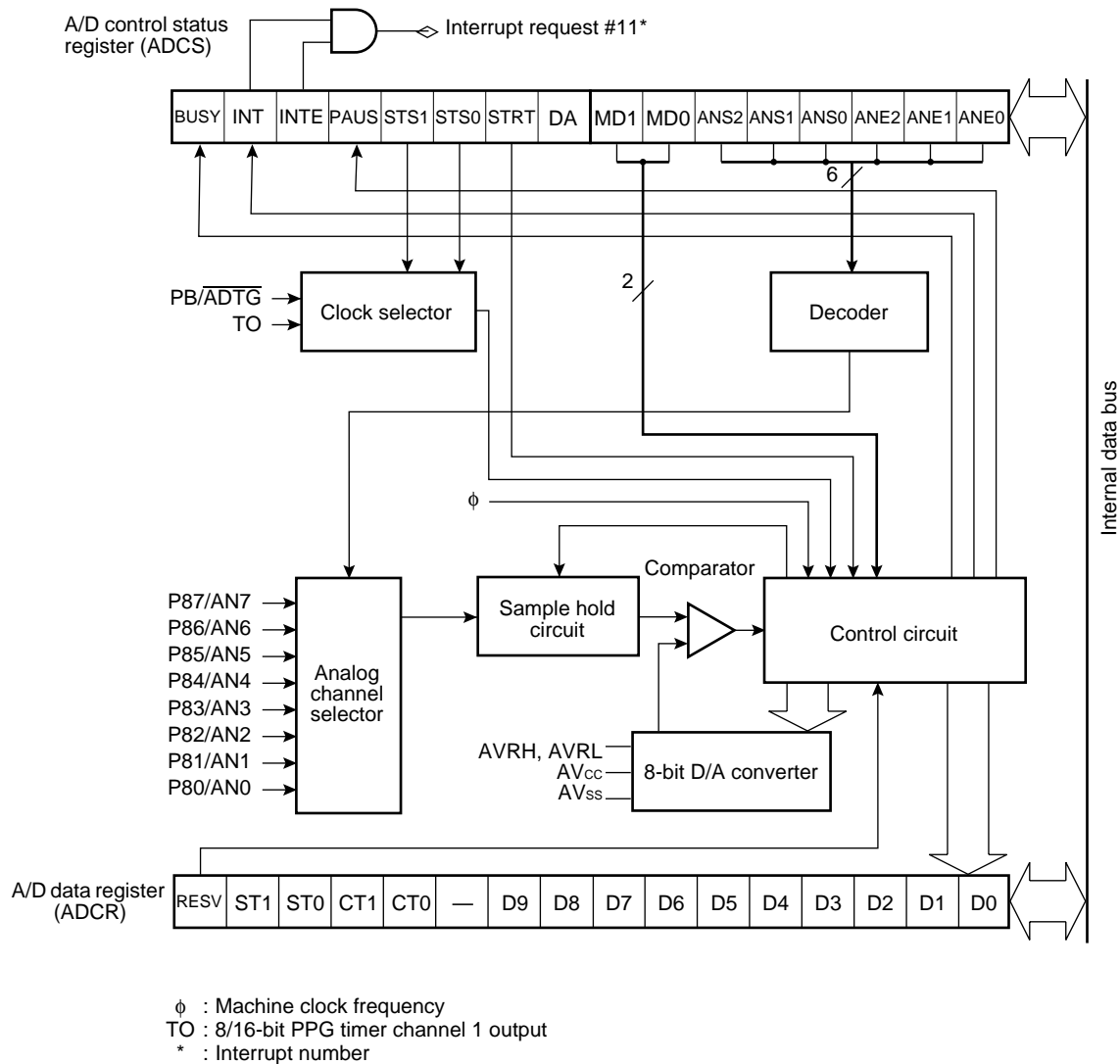
W : Write only

— : Reserved

X : Undefined

RESV : Reserved bit

(2) Block Diagram



MB90570/A Series

13. 8-bit D/A Converter

The 8-bit D/A converter, which is based on the R-2R system, supports 8-bit resolution mode. It contains two channels each of which can be controlled in terms of output by the D/A control register.

(1) Register Configuration

- D/A converter data register ch.0 (DADR0)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003A _H	(DADR1)			DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	XXXXXXXX _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- D/A converter data register ch.1 (DADR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00003B _H	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	(DADR0)			XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

- D/A control register 0 (DACR0)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003C _H	(DACR1)							—	—	—	DAE0	-----0 _B
								—	—	—	R/W	

- D/A control register 1 (DACR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00003D _H	—	—	—	—	—	—	—	DAE1	(DACR0)			-----0 _B
	—	—	—	—	—	—	—	R/W				

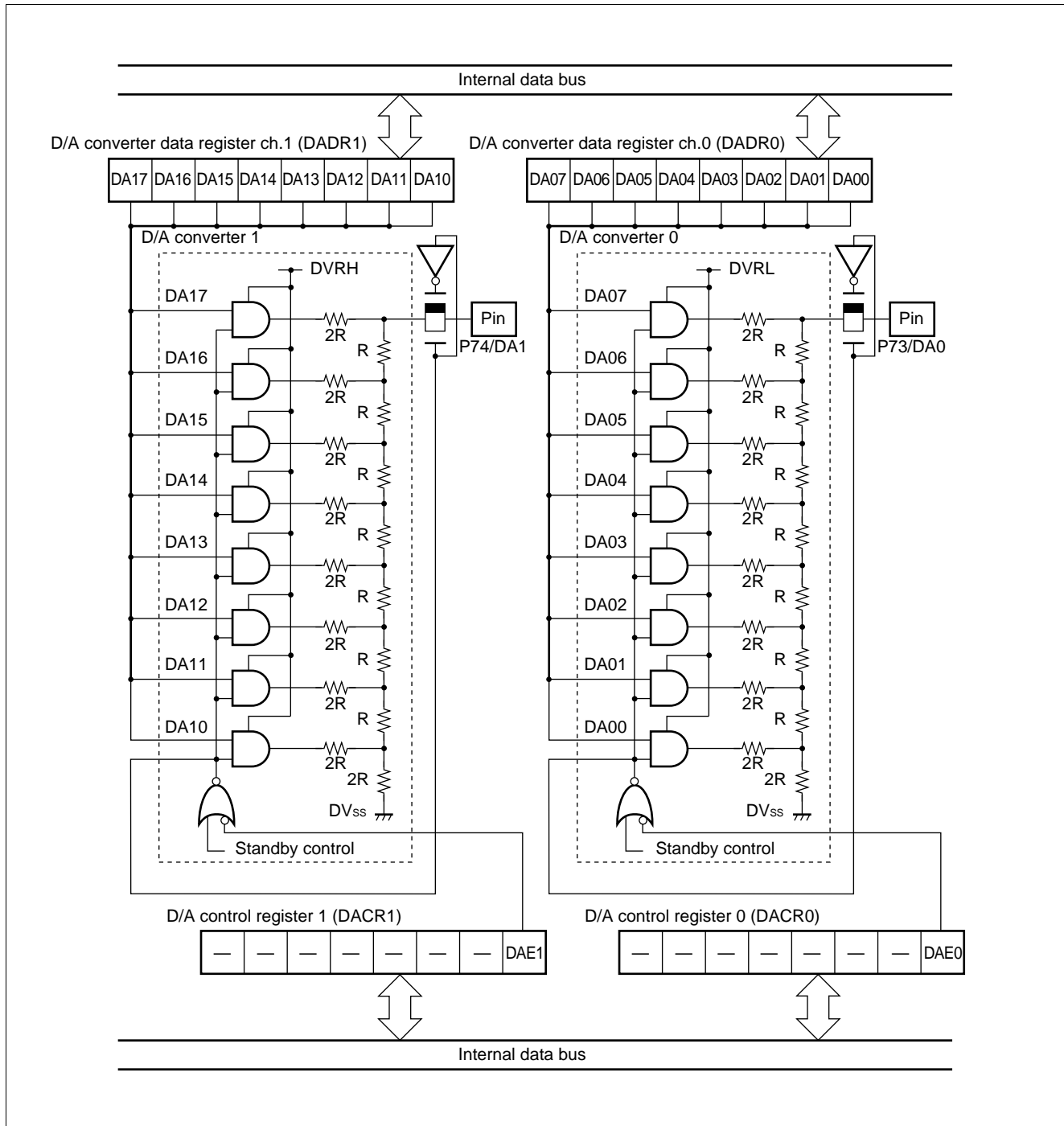
R/W: Readable and writable

— : Reserved

X : Undefined

MB90570/A Series

(2) Block Diagram



MB90570/A Series

14. Clock Timer

The clock timer control register (WTC) controls operation of the clock timer, and time for an interval interrupt.

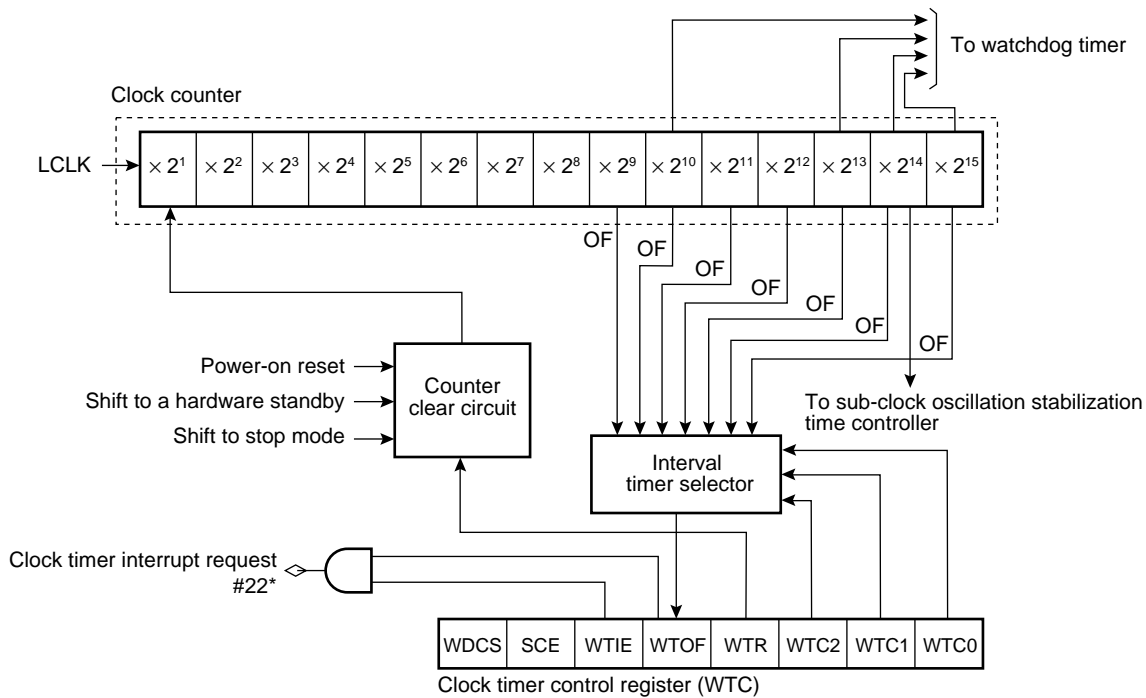
(1) Register Configuration

- Clock timer control register (WTC)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000AA _H	(Disabled)		WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	1X000000 _B
			R/W	R	R/W	R/W	R/W	R	R/W	R/W	

R/W: Readable and writable
R : Read only
X : Undefined

(2) Block Diagram



* : Interrupt number
OF : Overflow
LCLK : Oscillation sub-clock frequency

MB90570/A Series

15. Chip Select Output

This module generates a chip select signal for facilitating a memory and I/O unit, and is provided with eight chip select output pins. When access to an address is detected with a hardware-set area set for each pin register, a select signal is output from the pin.

(1) Register Configuration

- Chip selection control register 1, 3, 5, 7 (CSCR1, CSCR3, CSCR5, CSCR7)

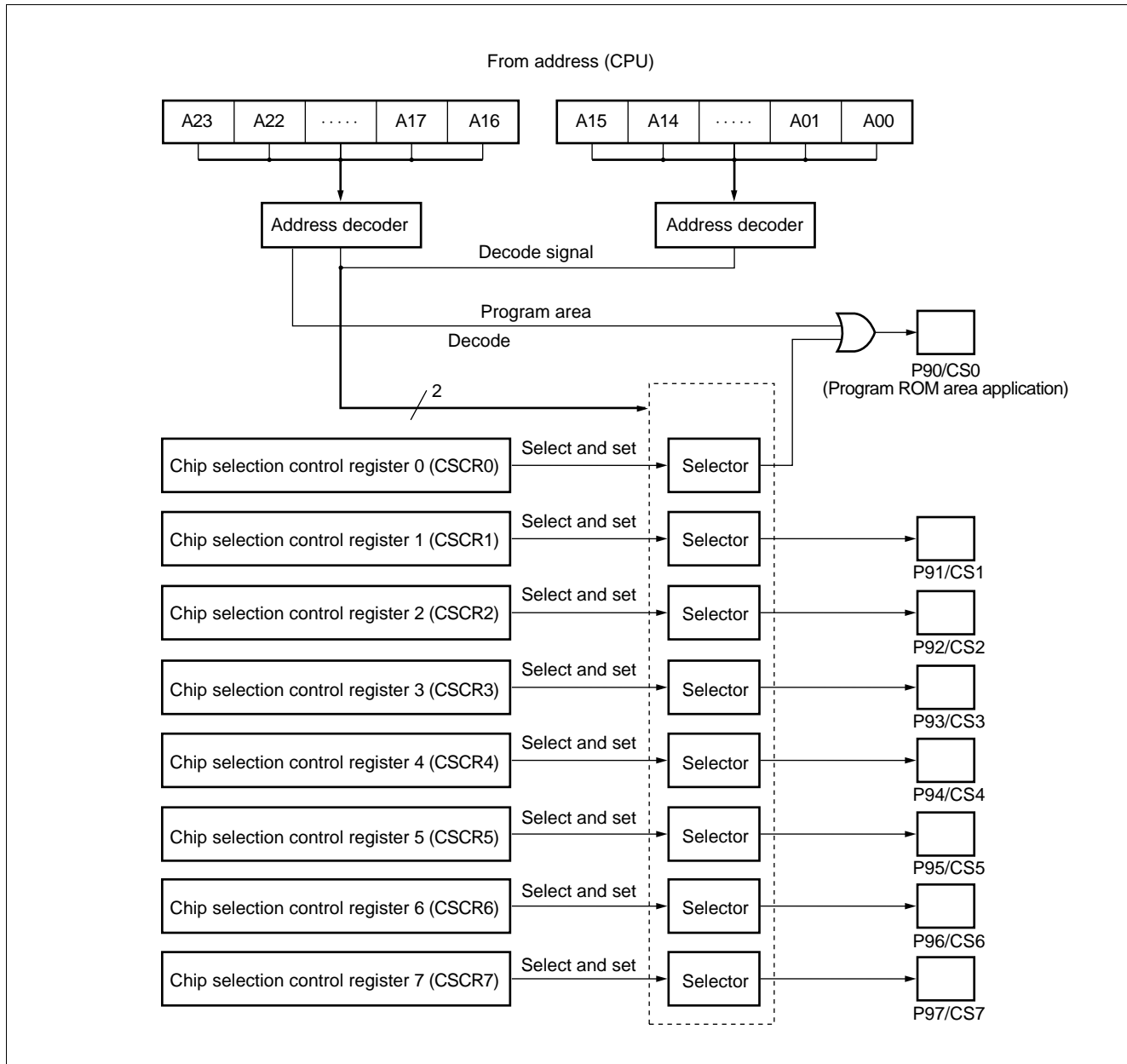
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0		
CSCR1 : 000081 _H	—	—	—	—	ACTL	OPEL	CSA1	CSA0	(CSCR0, CSCR2, CSCR4, CSCR6)				Initial value ----0000 _B
CSCR3 : 000083 _H	—	—	—	—	—	—	—	—	—				
CSCR5 : 000085 _H	—	—	—	—	—	—	—	—	—				
CSCR7 : 000087 _H	—	—	—	—	R/W	R/W	R/W	R/W	—				
- Chip selection control register 0, 2, 4, 6 (CSCR0, CSCR2, CSCR4, CSCR6)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
CSCR0 : 000080 _H	(CSCR1, CSCR3, CSCR5, CSCR7)			—	—	—	—	ACTL	OPEL	CSA1	CSA0	Initial value ----0000 _B
CSCR2 : 000082 _H	—			—	—	—	—	—	—	—		
CSCR4 : 000084 _H	—			—	—	—	—	—	—	—		
CSCR6 : 000086 _H	—			—	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable
— : Reserved

MB90570/A Series

(2) Block Diagram



MB90570/A Series

(3) Decode Address Spaces

Pin name	CSA		Decode space	Number of area bytes	Remarks
	1	0			
CS0	0	0	F00000 _H to FFFFFFF _H	1 Mbyte	Becomes active when the program ROM area or the program vector is fetched.
	0	1	F80000 _H to FFFFFFF _H	512 Kbyte	
	1	0	FE0000 _H to FFFFFFF _H	128 Kbyte	
	1	1	—	Disabled	
CS1	0	0	E00000 _H to EFFFFFF _H	1 Mbyte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	F00000 _H to F7FFFF _H	512 Kbyte	
	1	0	FC0000 _H to FFFFFFF _H	128 Kbyte	
	1	1	68FF80 _H to 68FFFF _H	128 byte	
CS2	0	0	003000 _H to 003FFF _H	4 Kbyte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	FA0000 _H to FBFFFF _H	128 Kbyte	
	1	0	68FF80 _H to 68FFFF _H	128 byte	
	1	1	68FF00 _H to 68FF7F _H	128 byte	
CS3	0	0	F80000 _H to F9FFFF _H	128 Kbyte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	68FF00 _H to 68FF7F _H	128 byte	
	1	0	68FE80 _H to 68FEFF _H	128 byte	
	1	1	—	Disabled	
CS4	0	0	002800 _H to 002FFF _H	2 Kbyte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	68FE80 _H to 68FEFF _H	128 byte	
	1	0	—	Disabled	
	1	1	—	Disabled	
CS5	0	0	68FF80 _H to 68FFFF _H	128 byte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	—	Disabled	
	1	0	—	Disabled	
	1	1	—	Disabled	
CS6	0	0	68FF00 _H to 68FF7F _H	128 byte	Adapted to the data ROM and RAM areas, and external circuit connection applications.
	0	1	—	Disabled	
	1	0	—	Disabled	
	1	1	—	Disabled	
CS7	—	—	—	Disabled	Disabled

MB90570/A Series

16. Communications Prescaler Register

This register controls machine clock division.

Output from the communications prescaler register is used for UART0 (SCI), UART1 (SCI), and extended I/O serial interface.

The communications prescaler register is so designed that a constant baud rate may be acquired for various machine clocks.

(1) Register Configuration

- Communications prescaler control register 0,1 (CDCR0, CDCR1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000028 _H	(Disabled)		MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0 - - - 1 1 1 1 _B
00002A _H			R/W	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable
— : Reserved

MB90570/A Series

17. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit and flag are prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at "1", the interrupt flag is set at "1" and the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code. The interrupt flag is cleared to "0" by writing "0" by an instruction.

(1) Register Configuration

- Program address detection register 0 to 2 (PADR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Low order address) : 001FF0 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Middle order address) : 001FF1 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (High order address) : 001FF2 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 3 to 5 (PADR1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Low order address) : 001FF3 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Middle order address) : 001FF4 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (High order address) : 001FF5 _H									XXXXXXXX _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

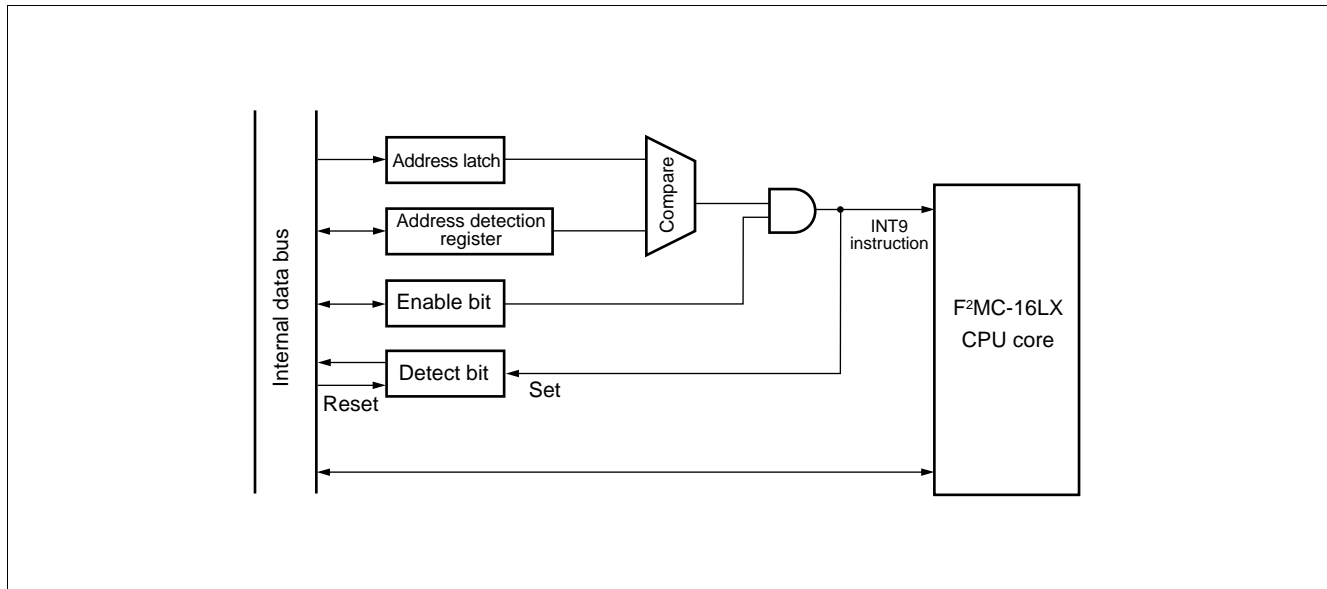
- Program address detection control status register (PACSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00009E _H	RESV	RESV	RESV	RESV	AD1E	AD1D	AD0E	AD0D	00000000 _B
	—	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 — : Reserved
 X : Undefined
 RESV : Reserved bit

MB90570/A Series

(2) Block Diagram



MB90570/A Series

18. ROM Mirroring Function Selection Module

The ROM mirroring function selection module can select what the FF bank allocated the ROM sees through the 00 bank according to register settings.

(1) Register Configuration

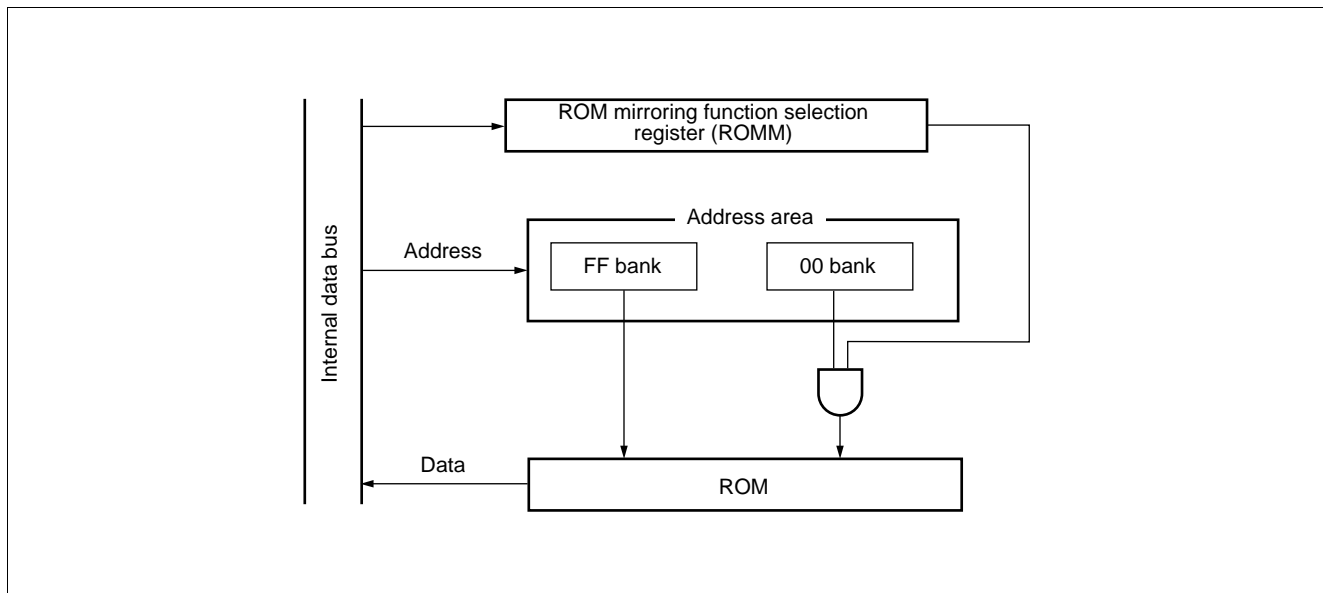
- ROM mirroring function selection register (ROMM)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00006FH	—	—	—	—	—	—	—	MI	(Disabled)			----- 1 _B
	—	—	—	—	—	—	—	W				

W : Write only
— : Reserved

Note: Do not access this register during operation at addresses 004000_H to 00FFFF_H.

(2) Block Diagram



MB90570/A Series

19. Low-power Consumption (Standby) Mode

The F²MC-16LX has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- **Clock mode**

PLL clock mode: A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock (HCLK).

Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscillation clock (HCLK).

The PLL multiplication circuits stops in the main clock mode.

- **CPU intermittent operation mode**

The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high-speed.

- **Hardware standby mode**

The hardware standby mode is a mode for reducing power consumption by stopping clock supply to the CPU by the low-power consumption control circuit, stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware standby mode). Of these modes, modes other than the PLL clock mode are power consumption modes.

(1) Register Configuration

- **Clock select register (CKSCR)**

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
0000A1 _H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	(LPMCR)			11111100 _B
	R	R	R/W	R/W	R/W	R/W	R/W	R/W				

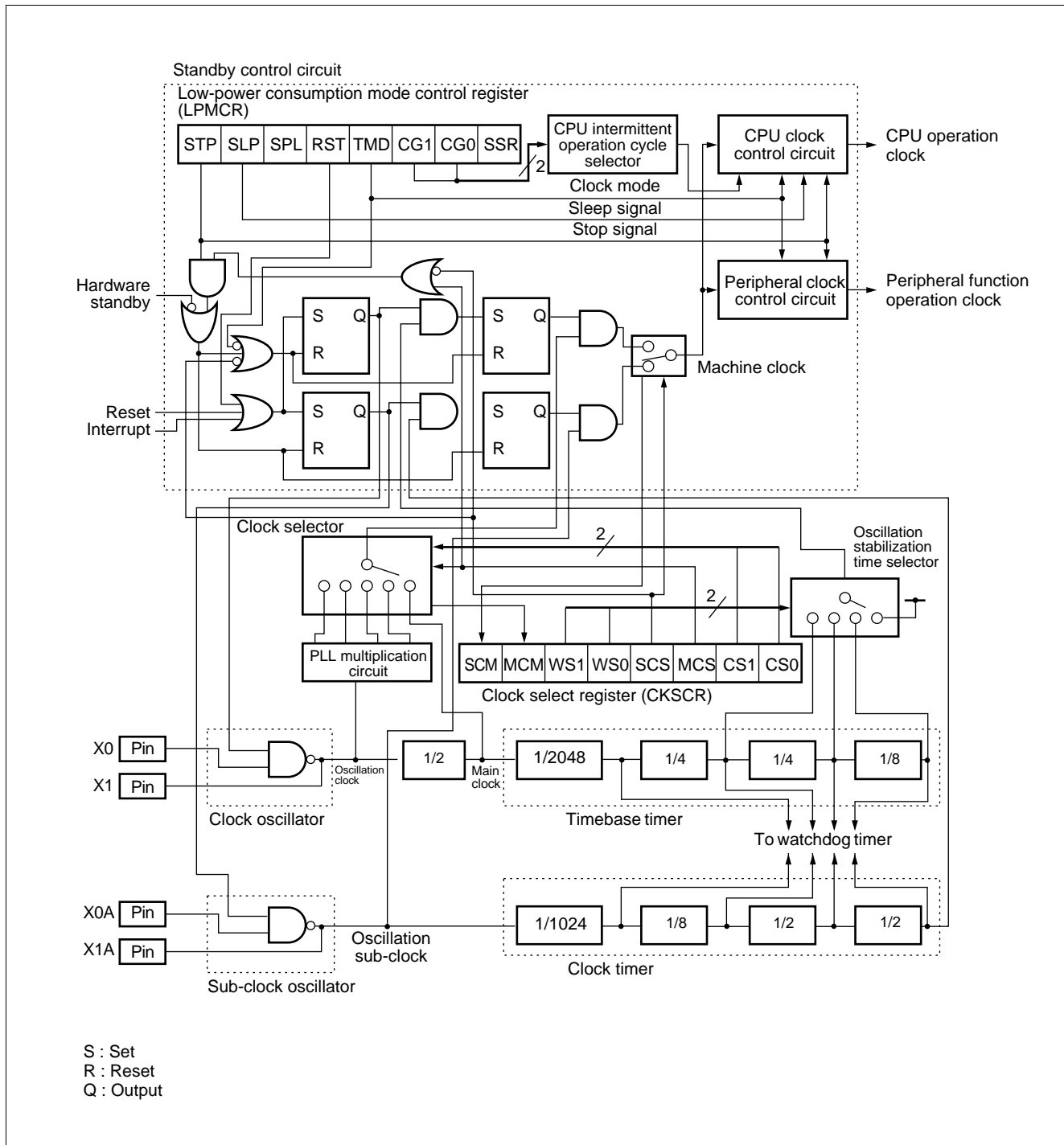
- **Low-power consumption mode control register (LPMCR)**

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A0 _H	(CKSCR)			STP	SLP	SPL	RST	TMD	CG1	CG0	SSR	00011000 _B
				W	W	R/W	W	R/W	W	R/W	R/W	

R/W: Readable and writable
 R : Read only
 W : Write only

MB90570/A Series

(2) Block Diagram



MB90570/A Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	*1
	AVRH, AVRL	V _{SS} – 0.3	V _{SS} + 6.0	V	*1
	DVRH	V _{SS} – 0.3	V _{SS} + 6.0	V	*1
Input voltage	V _I	V _{SS} – 0.3	V _{SS} + 6.0	V	*2
Output voltage	V _O	V _{SS} – 0.3	V _{SS} + 6.0	V	*2
“L” level maximum output current	I _{OL}	—	15	mA	*3
“L” level average output current	I _{OLAV}	—	4	mA	*4
“L” level total maximum output current	ΣI _{OL}	—	100	mA	
“L” level total average output current	ΣI _{OLAV}	—	50	mA	*5
“H” level maximum output current	I _{OH}	—	–15	mA	*3
“H” level average output current	I _{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI _{OH}	—	–100	mA	
“H” level total average output current	ΣI _{OHAV}	—	–50	mA	*5
Power consumption	P _D	—	300	mW	MB90573/4 MB90V570/A
		—	500	mW	MB90574A
		—	800	mW	MB90F574/A
Operating temperature	T _A	–40	+85	°C	
Storage temperature	T _{stg}	–55	+150	°C	

*1: AV_{CC}, AVRH, AVRL, and DVRH shall never exceed V_{CC}. AVRL shall never exceed AVRH.

*2: V_I and V_O shall never exceed V_{CC} + 0.3 V.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90570/A Series

2. Recommended Operating Conditions

($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90574/A)
	V_{CC}	4.5	5.5	V	Normal operation (MB90F574/A)
	V_{CC}	3.0	5.5	V	Retains status at the time of operation stop
Smoothing capacitor	C_S	0.1	1.0	μF	*
Operating temperature	T_A	-40	+85	$^{\circ}\text{C}$	

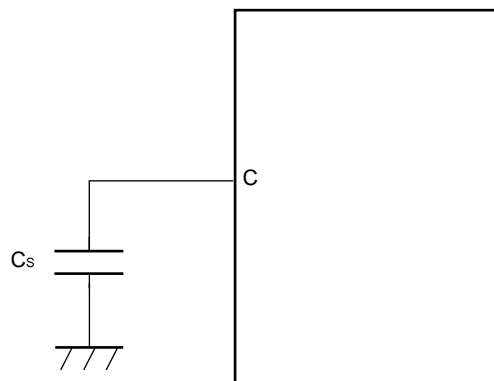
* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• C pin connection circuit



MB90570/A Series

3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IH}	CMOS input pin	$V_{CC} = 3.0 \text{ V}$ to 5.5 V (MB90573) (MB90574) $V_{CC} = 4.5 \text{ V}$ to 5.5 V (MB90F574)	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	CMOS hysteresis input pin		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHM}	MD pin input		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{IL}	CMOS input pin		$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	CMOS hysteresis input pin		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{ILM}	MD pin input		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
“H” level output voltage	V_{OH}	Other than PA6 and PA7	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -2.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL}	All output pins	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 2.0 \text{ mA}$	—	—	0.4	V	
Open-drain output leakage current	I_{leak}	PA6, PA7	—	—	0.1	5	μA	
Input leakage current	I_{IL}	Other than PA6 and PA7	$V_{CC} = 5.5 \text{ V}$ $V_{SS} < V_i < V_{CC}$	-5	—	5	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P60 to P67, RST, MD0, MD1	—	15	30	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD0 to MD2	—	15	30	100	$\text{k}\Omega$	
Power supply current*	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	30	40	mA	MB90574
	I_{CC}	V_{CC}		—	85	130	mA	MB90F574/A
	I_{CC}	V_{CC}		—	50	80	mA	MB90574A
	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V	—	35	45	mA	MB90574
	I_{CC}	V_{CC}		—	90	140	mA	MB90F574/A
	I_{CC}	V_{CC}		—	55	85	mA	MB90574A
	I_{CC}	V_{CC}	A/D converter operation	—	40	50	mA	MB90574
	I_{CC}	V_{CC}		—	95	145	mA	MB90F574/A
	I_{CC}	V_{CC}		—	60	90	mA	MB90574A

(Continued)

MB90570/A Series

(Continued)

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I _{CC}	V _{CC}	When data written in flash mode programming of erasing	—	95	140	mA	MB90F574/A
	I _{CCS}	V _{CC}	Internal operation at 16 MHz V _{CC} = 5.0 V In sleep mode	—	7	12	mA	MB90574
	I _{CCS}	V _{CC}		—	5	10	mA	MB90F574/A
	I _{CCS}	V _{CC}		—	15	20	mA	MB90574A
	I _{CCCL}	V _{CC}	Internal operation at 8 kHz V _{CC} = 5.0 V T _A = +25°C Subsystem operatin	—	0.1	1.0	mA	MB90574
	I _{CCCL}	V _{CC}		—	4	7	mA	MB90F574/A
	I _{CCCL}	V _{CC}		—	0.03	1	mA	MB90574A
	I _{CCCLS}	V _{CC}	Internal operation at 8 kHz V _{CC} = 5.0 V T _A = +25°C In subsleep mode	—	30	50	mA	MB90574
	I _{CCCLS}	V _{CC}		—	0.1	1	mA	MB90F574/A
	I _{CCCLS}	V _{CC}		—	10	50	μA	MB90574A
	I _{CCCT}	V _{CC}	Internal operation at 8 kHz V _{CC} = 5.0 V T _A = +25°C In clock mode	—	15	30	μA	MB90574
	I _{CCCT}	V _{CC}		—	30	50	μA	MB90F574/A
	I _{CCCT}	V _{CC}		—	1.0	30	μA	MB90574A
	I _{CCCH}	V _{CC}	T _A = +25°C In stop mode	—	5	20	μA	MB90574
	I _{CCCH}	V _{CC}		—	0.1	10	μA	MB90F574/A MB90574A
Input capacitance	C _{IN}	Other than AV _{CC} , AV _{SS} , V _{CC} , V _{SS}	—	—	10	80	pF	

* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice.

MB90570/A Series

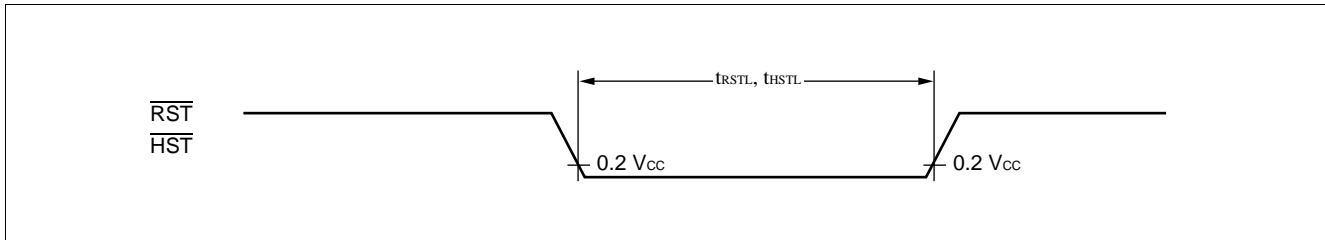
4. AC Characteristics

(1) Reset, Hardware Standby Input Timing

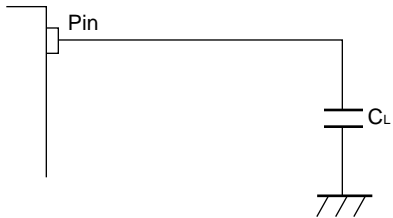
($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	\overline{RST}	—	$4\ t_{CP}^*$	—	ns	
Hardware standby input time	t_{HSTL}	\overline{HST}		$4\ t_{CP}^*$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



• Measurement conditions for AC characteristics



C_L is a load capacitance connected to a pin under test.

Capacitors of $C_L = 30\text{ pF}$ must be connected to CLK and ALE pins, while C_L of 80 pF must be connected to address data bus (AD15 to AD00), \overline{RD} , and \overline{WR} pins.

MB90570/A Series

(2) Specification for Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

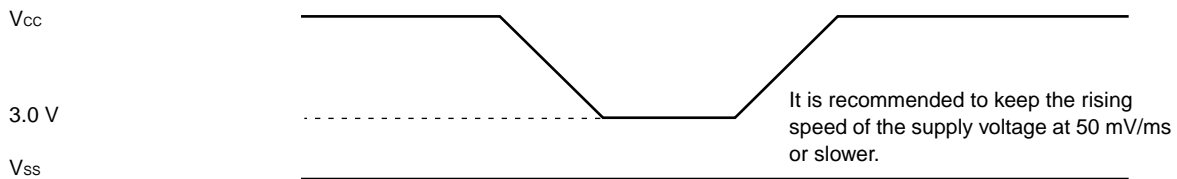
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}		4	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

- Notes:
- The above ratings are values for causing a power-on reset.
 - There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.



Sudden changes in the power supply voltage may cause a power-on reset. To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below. In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 mV or fewer per second, however, you can use the PLL clock.



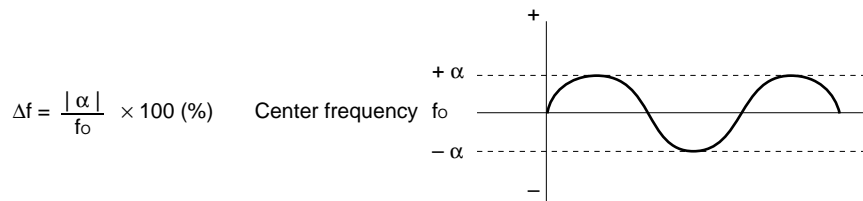
MB90570/A Series

(3) Clock Timings

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		62.5	—	333	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0		10	—	—	ns	Recommended duty ratio of 30% to 70%
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	μs	
Input clock rising/falling time	t_{CR}, t_{CF}	X0, X0A		—	—	5	ns	External clock operation
Internal operating clock frequency	f_{CP}	—		1.5	—	16	MHz	Main clock operation
	f_{LCP}	—		—	8.192	—	kHz	Subclock operation
Internal operating clock cycle time	t_{CP}	—		62.5	—	333	ns	External clock operation
	t_{LCP}	—		—	122.1	—	μs	Subclock operation
Frequency fluctuation rate locked	Δf	—		—	—	5	%	*

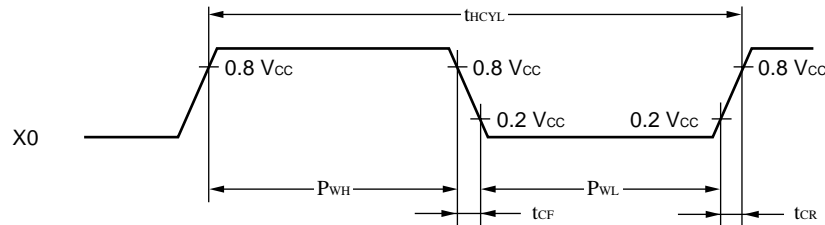
* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.



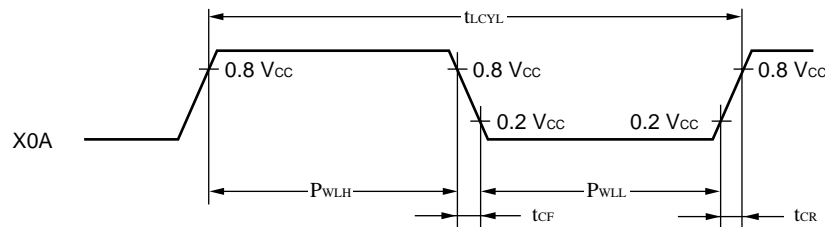
The PLL frequency deviation changes periodically from the preset frequency “(about $CLK \times (1CYC$ to $50CYC)$ ”, thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

MB90570/A Series

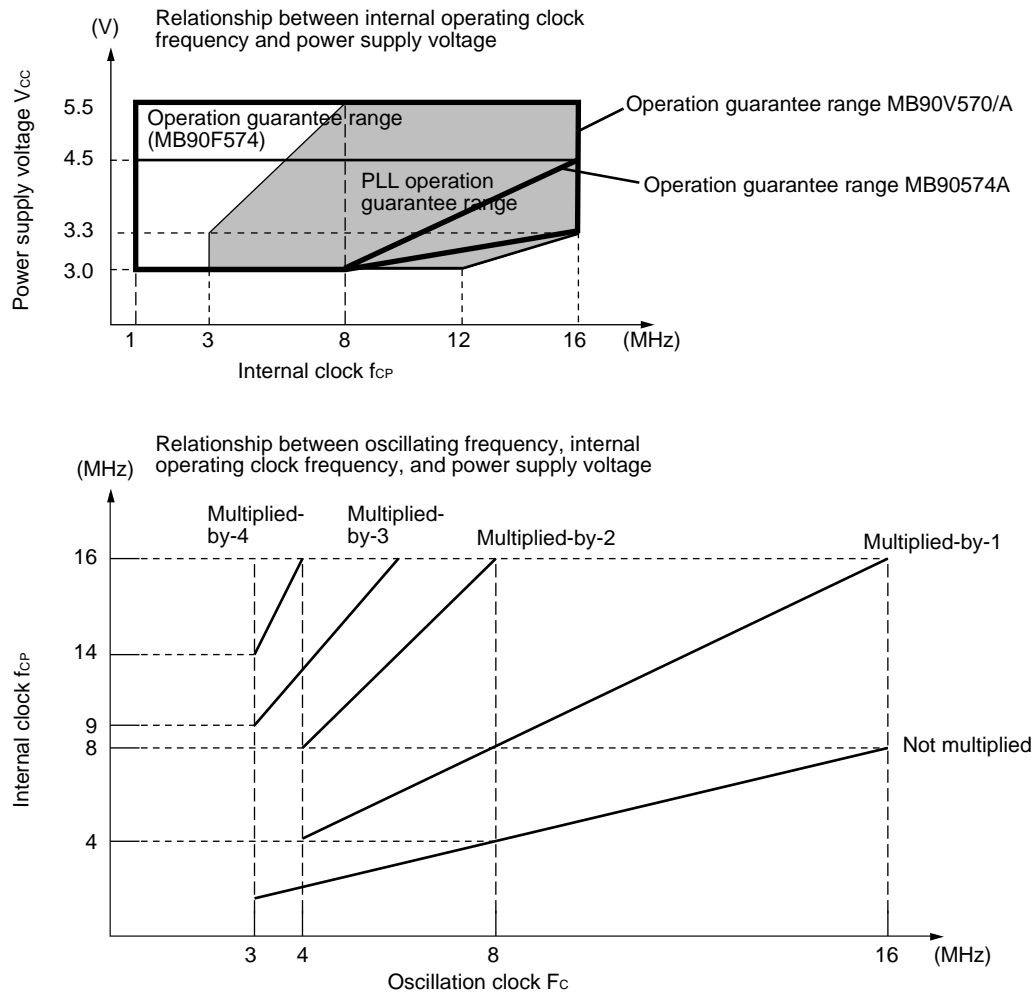
• X0, X1 clock timing



• X0A, X1A clock timing



• PLL operation guarantee range

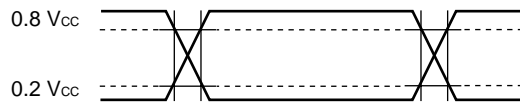


MB90570/A Series

The AC ratings are measured for the following measurement reference voltages.

• Input signal waveform

Hysteresis input pin

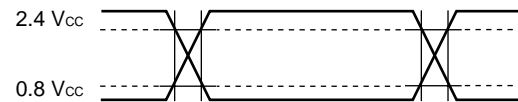


Pins other than hysteresis input/MD input



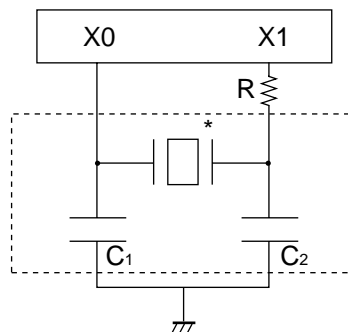
• Output signal waveform

Hysteresis input pin



(4) Recommended Resonator Manufacturers

• Sample application of ceramic resonator



• Mask ROM product (MB90574)

Resonator manufacturer*	Resonator	Frequency (MHz)	C ₁ (pF)	C ₁ (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	No required
	CSA4.00MG040	4.00	100	100	No required
	CSA8.00MTZ	8.00	30	30	No required
	CSA16.00MXZ040	16.00	15	15	No required
	CSA32.00MXZ040	32.00	5	5	No required
TDK Coporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	No required
	CCR7.0MC5 to CCR12.0MC5	7.00 to 12.00	Built-in	Built-in	No required
	CCR20.0MSC6 to CCR32.0MSC6	20.00 to 32.00	Built-in	Built-in	No required

(Continued)

MB90570/A Series

(Continued)

- Flash product (MB90F574)

Resonator manufacturer*	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	No required
	CSA4.00MG040	4.00	100	100	No required
	CSA8.00MTZ	8.00	30	30	No required
	CSA16.00MXZ040	16.00	15	15	No required
	CSA32.00MXZ040	32.00	5	5	No required
TDK Coporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	No required
	CCR7.0MC5 to CCR12.0MC5	7.00 to 12.00	Built-in	Built-in	No required
	CCR20.0MSC6 to CCR32.0MSC6	20.00 to 32.00	Built-in	Built-in	No required

Inquiry: Murata Mfg. Co., Ltd..

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.): TEL 65-758-4233

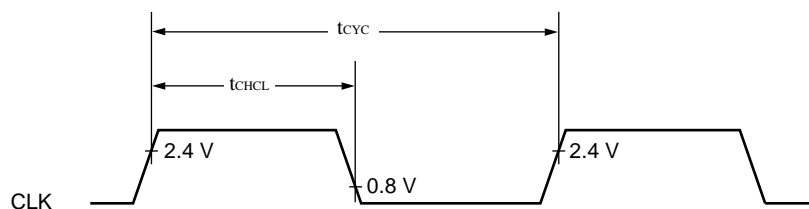
TDK Corporation

- TDK Corporation of America
Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH
Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hongkong Co., Ltd.: TEL: 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6636

(5) Clock Output Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t _{CYC}	CLK	—	62.5	—	ns	
CLK ↑ → CLK ↓	t _{CHCL}	CLK		20	—	ns	



MB90570/A Series

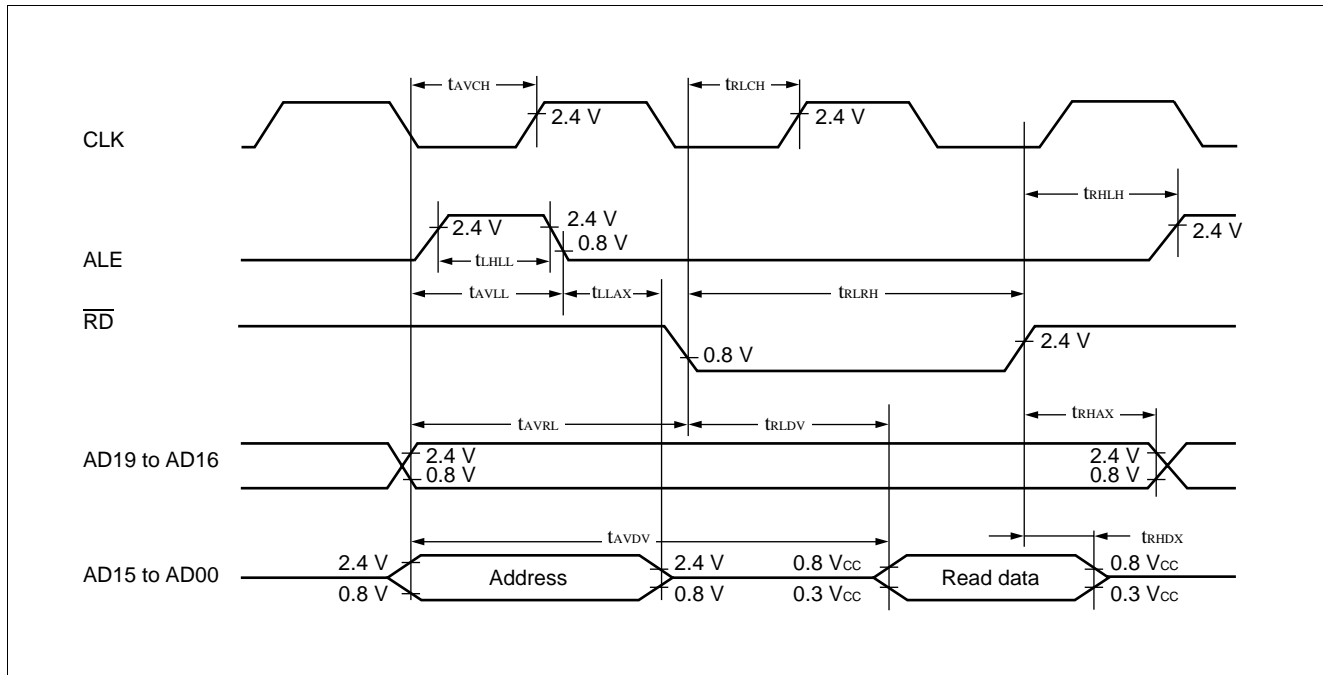
(6) Bus Read Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t _{LHLL}	ALE	—	1 t _{CP} */2 - 20	—	ns	
Effective address → ALE ↓ time	t _{AVLL}	ALE, A23 to A16, AD15 to AD00		1 t _{CP} */2 - 20	—	ns	
ALE ↓ → address effective time	t _{LLAX}	ALE, AD15 to AD00		1 t _{CP} */2 - 15	—	ns	
Effective address → $\overline{\text{RD}}$ ↓ time	t _{AVRL}	$\overline{\text{RD}}$, A23 to A16, AD15 to AD00		1 t _{CP} * - 15	—	ns	
Effective address → valid data input	t _{AVDV}	A23 to A16, AD15 to AD00		—	5 t _{CP} */2 - 60	ns	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	$\overline{\text{RD}}$		3 t _{CP} */2 - 20	—	ns	
$\overline{\text{RD}}$ ↓ → valid data input	t _{RLDV}	$\overline{\text{RD}}$, AD15 to AD00		—	3 t _{CP} */2 - 60	ns	
$\overline{\text{RD}}$ ↑ → data hold time	t _{RHDX}	$\overline{\text{RD}}$, AD15 to AD00		0	—	ns	
$\overline{\text{RD}}$ ↑ → ALE ↑ time	t _{RHLH}	ALE, $\overline{\text{RD}}$		1 t _{CP} */2 - 15	—	ns	
$\overline{\text{RD}}$ ↑ → address effective time	t _{RHAX}	ALE, A23 to A16		1 t _{CP} */2 - 10	—	ns	
Effective address → CLK ↑ time	t _{AVCH}	CLK, A23 to A16, AD15 to AD00		1 t _{CP} */2 - 20	—	ns	
$\overline{\text{RD}}$ ↓ → CLK ↑ time	t _{RLCH}	CLK, $\overline{\text{RD}}$		1 t _{CP} */2 - 20	—	ns	
ALE ↓ → $\overline{\text{RD}}$ ↓ time	t _{ALRL}	ALE, $\overline{\text{RD}}$		1 t _{CP} */2 - 15	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

MB90570/A Series



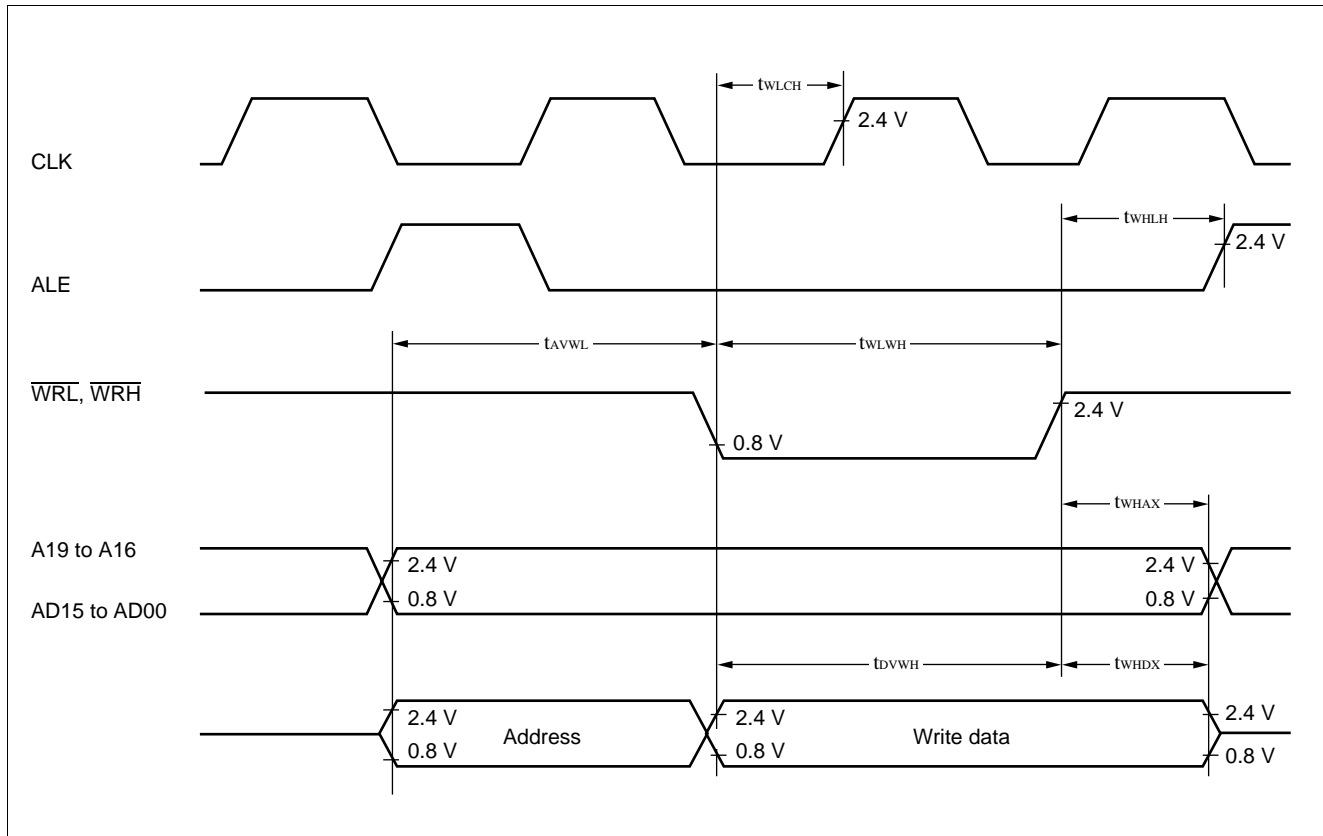
MB90570/A Series

(7) Bus Write Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Effective address $\rightarrow \overline{WR}$ \downarrow time	t_{AVWL}	\overline{WR} , A23 to A16, AD15 to AD00	—	$1\ t_{CP} - 15$	—	ns	
\overline{WR} pulse width	t_{WLWH}	\overline{WR}		$3\ t_{CP}^*/2 - 20$	—	ns	
Write data $\rightarrow \overline{WR}$ \uparrow time	t_{DVWH}	\overline{WR} , AD15 to AD00		$3\ t_{CP}^*/2 - 20$	—	ns	
\overline{WR} $\uparrow \rightarrow$ data hold time	t_{WHDX}	\overline{WR} , AD15 to AD00		20	—	ns	
\overline{WR} $\uparrow \rightarrow$ address effective time	t_{WHAX}	\overline{WR} , A23 to A16		$1\ t_{CP}^*/2 - 10$	—	ns	
\overline{WR} $\uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	ALE, \overline{WRL}		$1\ t_{CP}^*/2 - 15$	—	ns	
\overline{WR} $\downarrow \rightarrow$ CLK \uparrow time	t_{WLCH}	CLK, \overline{WRH}		$1\ t_{CP}^*/2 - 20$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



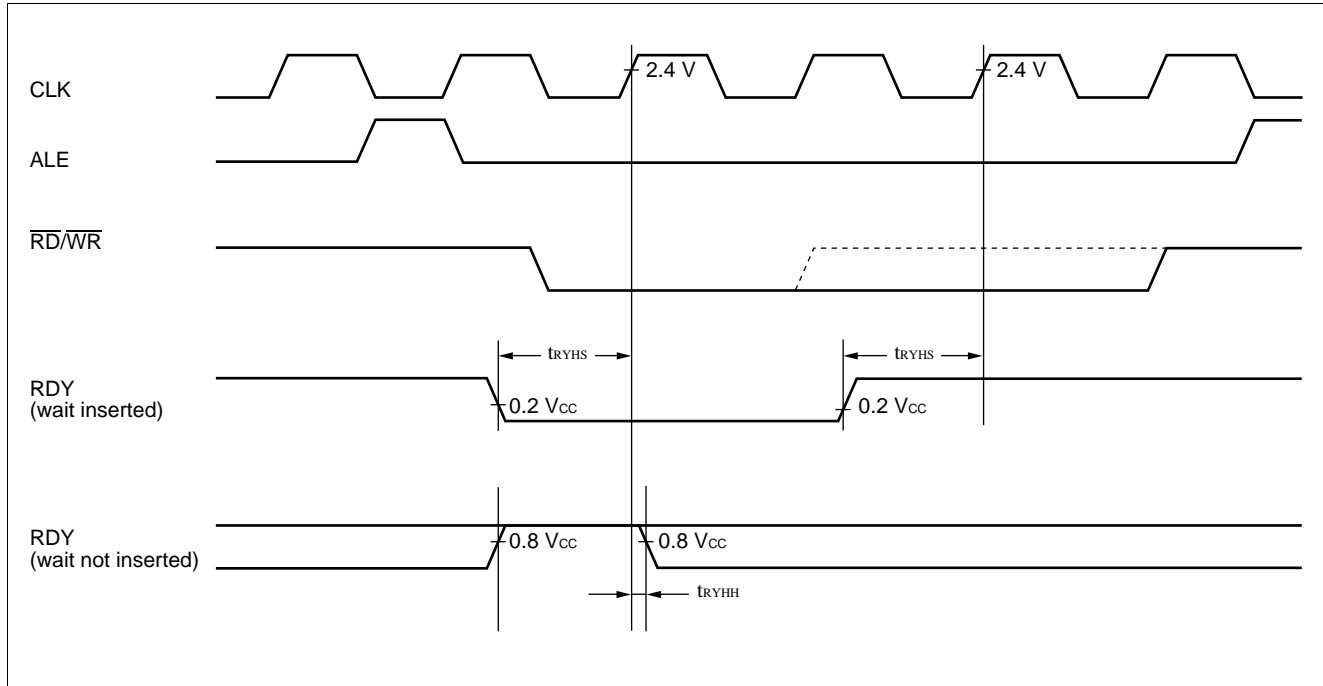
MB90570/A Series

(8) Ready Input Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: Use the automatic ready function when the setup time for the rising edge of the RDY signal is not sufficient.



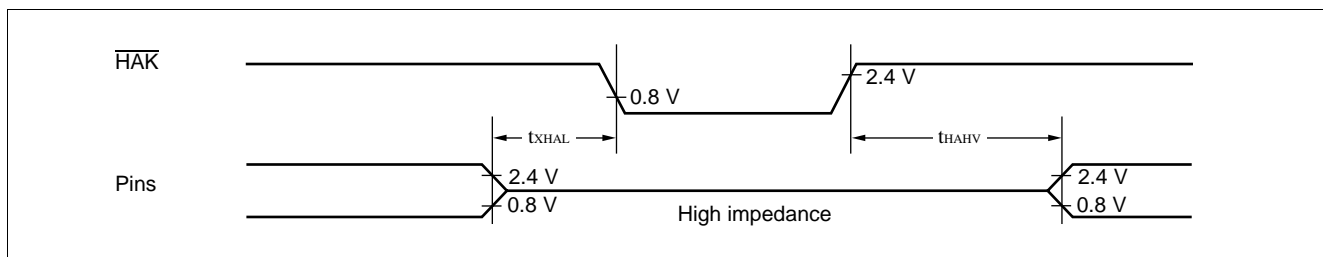
(9) Hold Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pins in floating status → $\overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	1 t_{CP}^*	ns	
$\overline{\text{HAK}} \uparrow \rightarrow$ pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		1 t_{CP}^*	2 t_{CP}^*	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

Note: More than 1 machine cycle is needed before $\overline{\text{HAK}}$ changes after HRQ pin is fetched.



MB90570/A Series

(10) UART0 (SCI), UART1 (SCI) Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal shift clock mode $C_L = 80\text{ pF}$ + 1 TTL for an output pin	$8\ t_{CP}^*$	—	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		– 80	80	ns	
Valid SIN \rightarrow SCK \uparrow	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		100	—	ns	
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK4	External shift clock mode $C_L = 80\text{ pF}$ + 1 TTL for an output pin	$4\ t_{CP}^*$	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK4		$4\ t_{CP}^*$	—	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		—	150	ns	
Valid SIN \rightarrow SCK \uparrow	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	

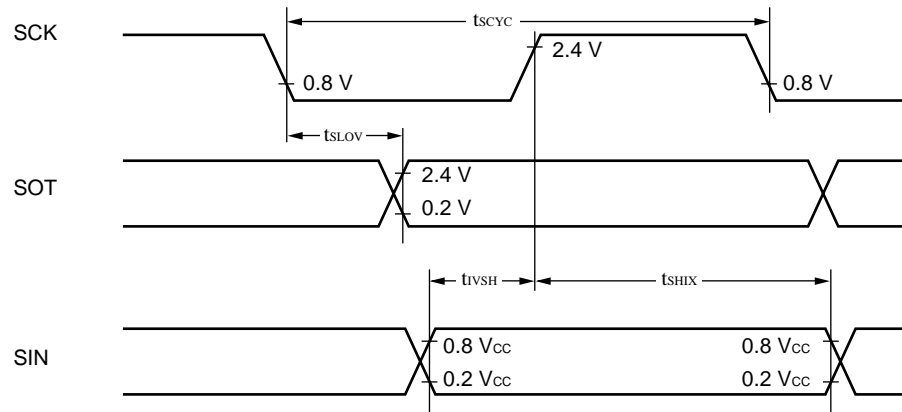
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

Notes: • These are AC ratings in the CLK synchronous mode.

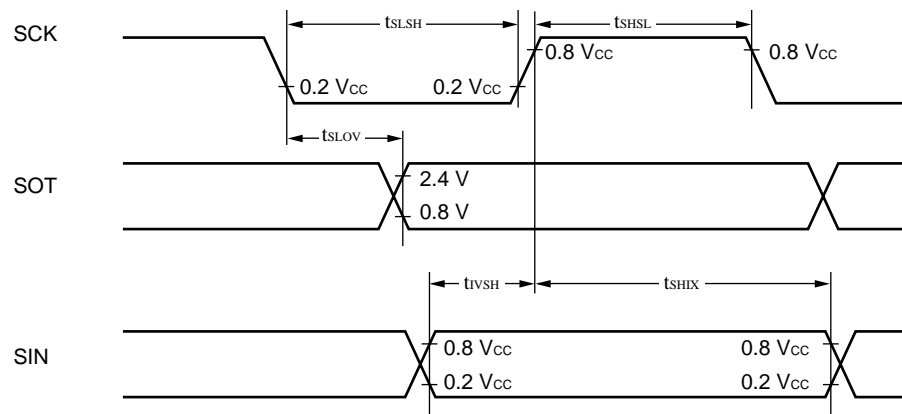
• C_L is the load capacitance value connected to pins while testing.

MB90570/A Series

- Internal shift clock mode



- External shift clock mode



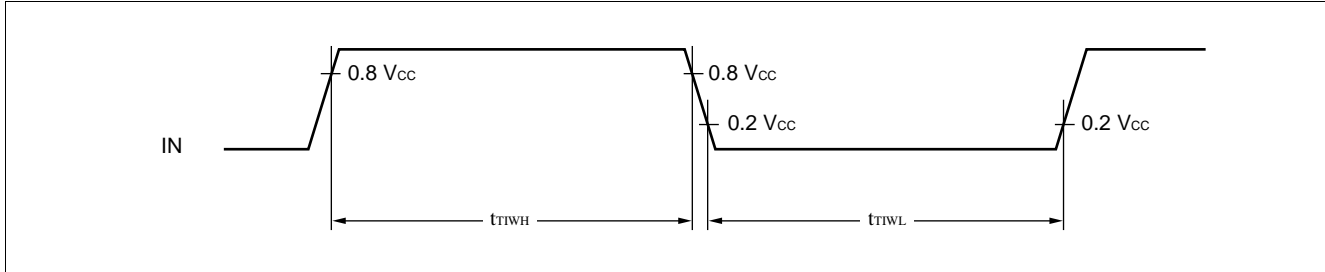
MB90570/A Series

(11) Timer Input Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} , t_{TIWL}	IN0, IN1	—	$4\ t_{CP}^*$	—	ns	

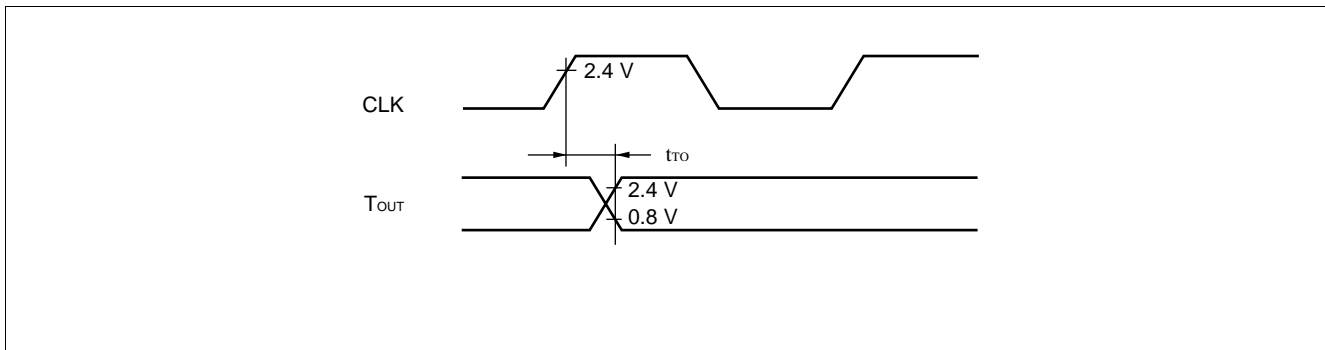
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



(12) Timer Output Timing

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK $\uparrow \rightarrow T_{OUT}$ transition time	t_{ro}	OUT0 to OUT3, PPG0, PPG1	—	30	—	ns	



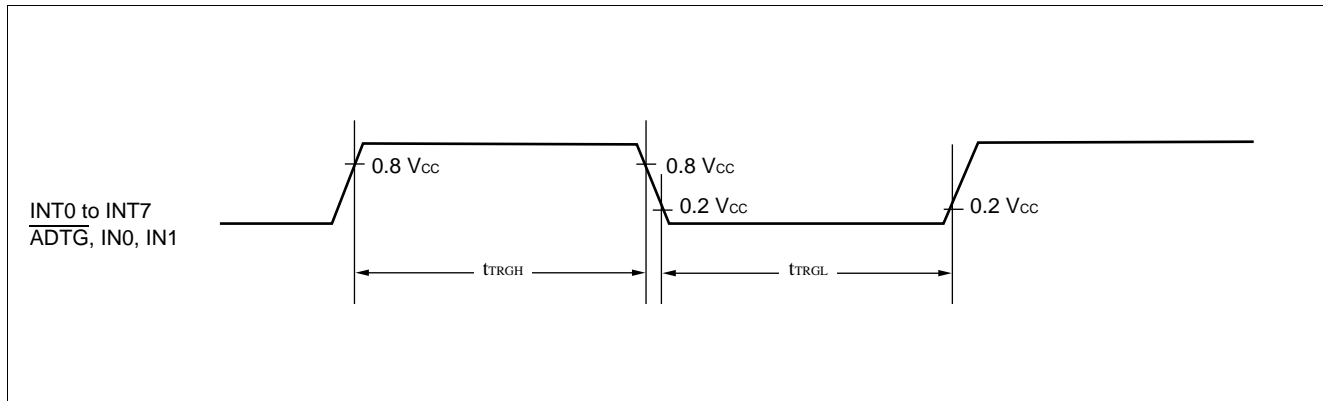
MB90570/A Series

(13) Trigger Input Timing

($AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7, ADTG, IN0, IN1	—	$5 t_{\text{CP}}^*$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



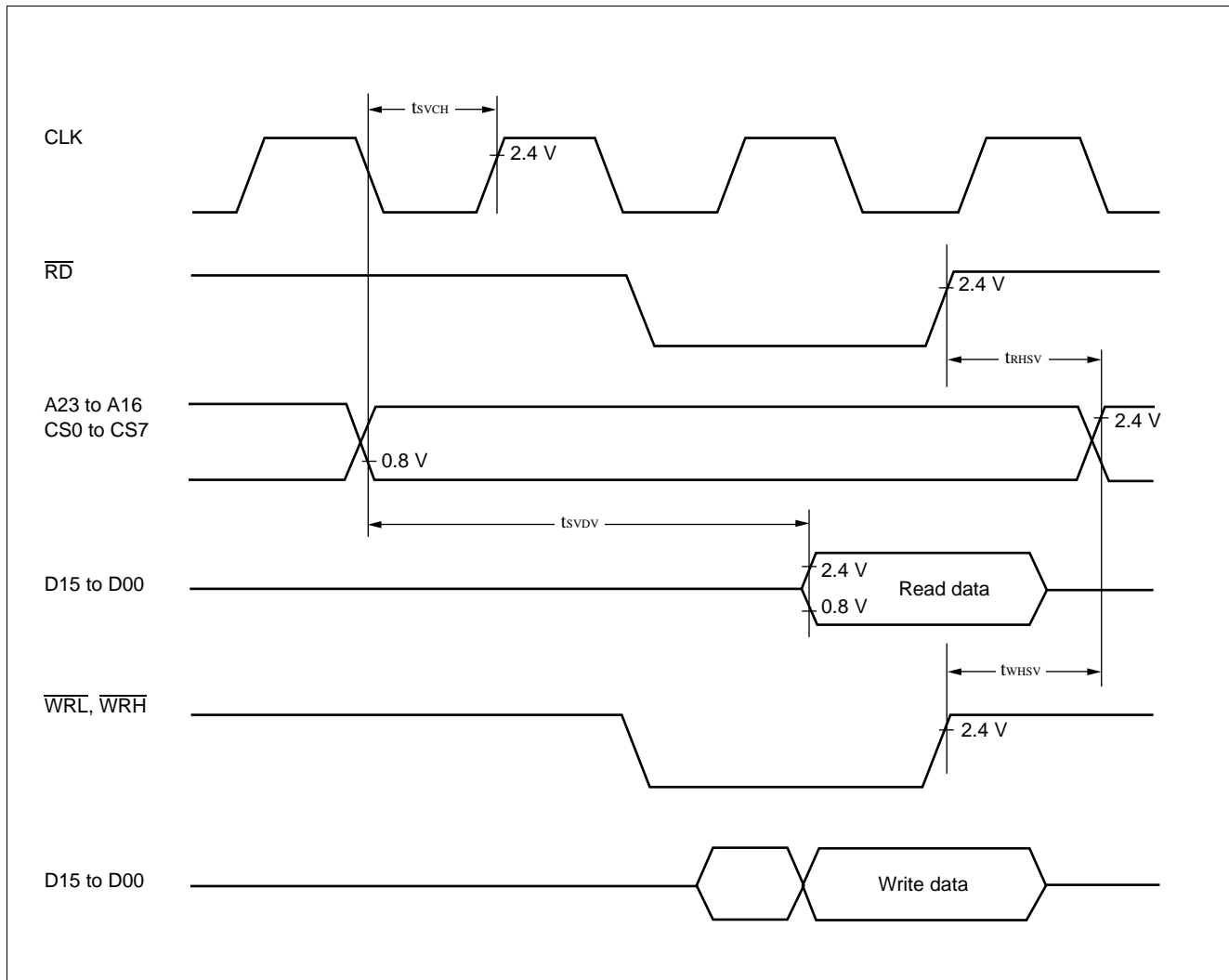
MB90570/A Series

(14) Chip Select Output Timing

($AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid chip select output → Valid data input time	t_{SVDV}	CS0 to CS7, D15 to D00	—	—	$5 t_{\text{CP}}^*/2 - 60$	ns	
$\overline{\text{RD}} \uparrow \rightarrow$ chip select output effective time	t_{RHSV}	$\overline{\text{RD}}$, CS0 to CS7		$1 t_{\text{CP}}^*/2 - 10$	—	ns	
$\overline{\text{WR}} \uparrow \rightarrow$ chip select output effective time	t_{WHSV}	CS0 to CS7, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$		$1 t_{\text{CP}}^*/2 - 10$	—	ns	
Valid chip select output → CLK \uparrow time	t_{SVCH}	CLK, CS0 to CS7		$1 t_{\text{CP}}^*/2 - 20$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



MB90570/A Series

(15) I²C Timing

($AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

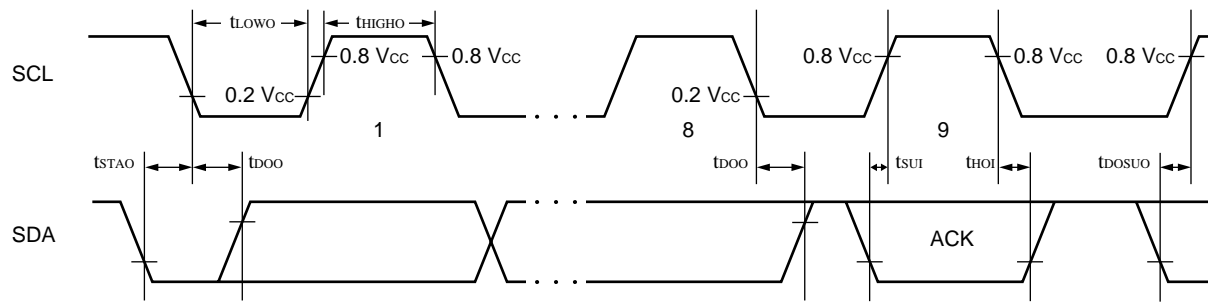
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Internal clock cycle time	t _{CP}	—	—	62.5	666	ns	All products
Start condition output	t _{STAO}	SDA0,SDA1 SCL0,SCL1		t _{CP} ×m×n/2-20	t _{CP} ×m×n/2+20	ns	Only as master
Stop condition output	t _{STOO}			t _{CP} (m×n/ 2+4)-20	t _{CP} (m×n/ 2+4)+20	ns	
Start condition detection	t _{STAI}			3t _{CP} +40	—	ns	Only as slave
Stop condition detection	t _{STOI}			3t _{CP} +40	—	ns	
SCL output “L” width	t _{LOWO}	SCL0,SCL1		t _{CP} ×m×n/2-20	t _{CP} ×m×n/2+20	ns	Only as master
SCL output “H” width	t _{HIGHO}			t _{CP} (m×n/ 2+4)-20	t _{CP} (m×n/ 2+4)+20	ns	
SDA output delay time	t _{DOO}	SDA0,SDA1 SCL0,SCL1		2t _{CP} -20	2t _{CP} +20	ns	
Setup after SDA output interrupt period	t _{DOSUO}			4t _{CP} -20	—	ns	
SCL input “L” width	t _{LOWI}	SCL0,SCL1		3t _{CP} +40	—	ns	
SCL input “H” width	t _{HIGHI}			t _{CP} +40	—	ns	
SDA input setup time	t _{SUI}	SDA0,SDA1 SCL0,SCL1		40	—	ns	
SDA input hold time	t _{HOI}			0	—	ns	

Notes: • “m” and “n” in the above table represent the values of shift clock frequency setting bits (CS4-CS0) in the clock control register “ICCR”. For details, refer to the register description in the hardware manual.

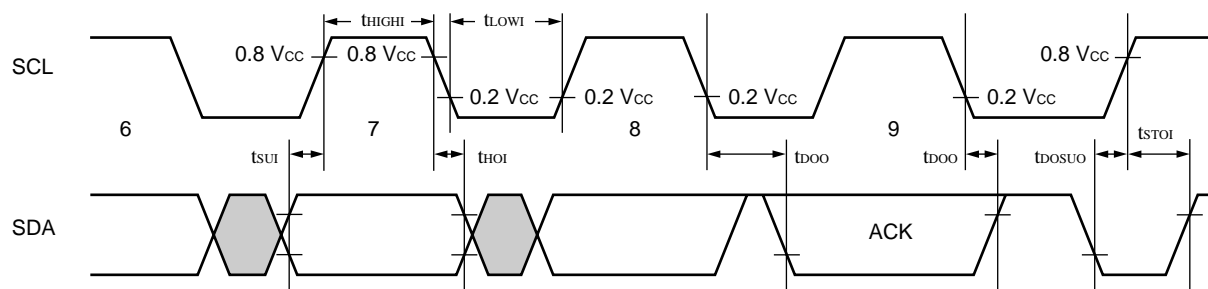
- t_{DOSUO} represents the minimum value when the interrupt period is equal to or greater than the SCL “L” width.
- The SDA and SCL output values indicate that that rise time is 0 ns.

MB90570/A Series

- I²C interface [data transmitter (master/slave)]



- I²C interface [data receiver (master/slave)]



MB90570/A Series

5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $2.7 \text{ V} \leq AVR_H - AVR_L$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution	—	—	—	—	8/10	—	bit
Total error	—	—		—	—	± 5.0	LSB
Non-linear error	—	—		—	—	± 2.5	LSB
Differential linearity error	—	—		—	—	± 1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN7		-3.5 LSB	+0.5 LSB	+4.5 LSB	mV
Full-scale transition voltage	V_{FST}	AN0 to AN7		AVRH -6.5 LSB	AVRH -1.5 LSB	AVRH +1.5 LSB	mV
Conversion time	—	—	$V_{CC} = 5.0 \text{ V} \pm 10\%$ at machine clock of 16 MHz	352 t_{CP}	—	—	μs
Sampling period	—	—	$V_{CC} = 5.0 \text{ V} \pm 10\%$ at machine clock of 6 MHz	64 t_{CP}	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN7	—	—	—	10	μA
Analog input voltage	V_{AIN}	AN0 to AN7		AVRL	—	AVRH	V
Reference voltage	—	AVRH		AVRL +2.7	—	AV_{CC}	V
	—	AVRL		0	—	AVRH -2.7	V
Power supply current	I_A	AV_{CC}		—	5	—	mA
	I_{AH}	AV_{CC}	CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC} = AV_{CC} = AVR_H = 5.0 \text{ V}$)	—	—	5	μA
Reference voltage supply current	I_R	AVRH	—	—	400	—	μA
	I_{RH}	AVRH	CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC} = AV_{CC} = AVR_H = 5.0 \text{ V}$)	—	—	5	μA
Offset between channels	—	AN0 to AN7	—	—	—	4	LSB

MB90570/A Series

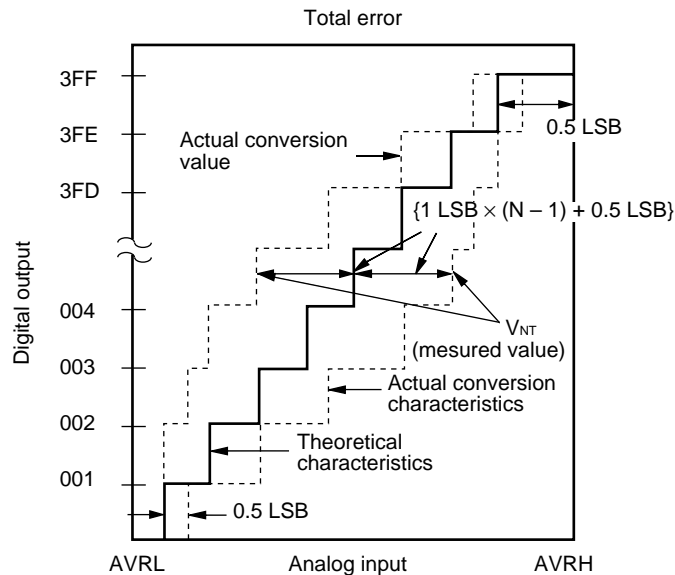
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB [V]}$$

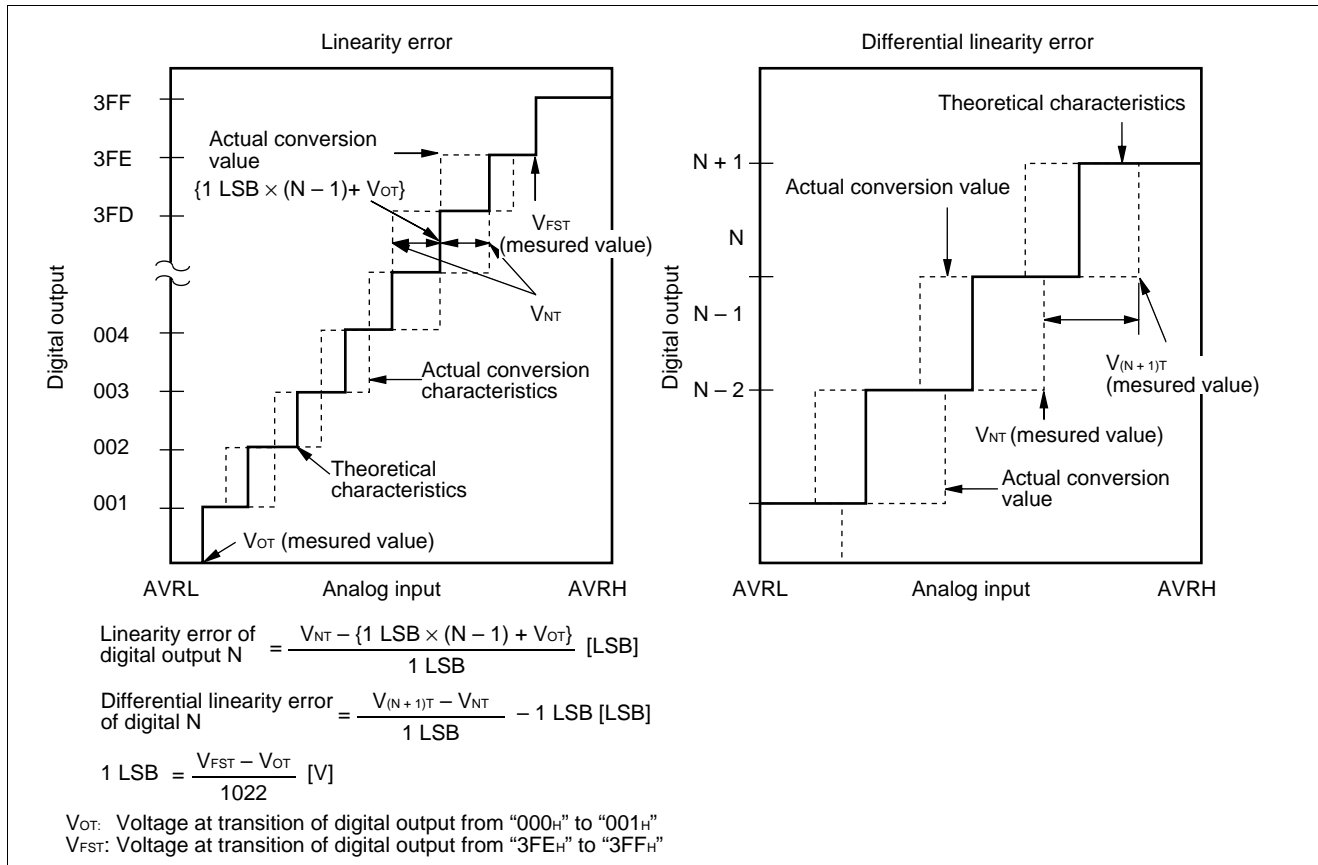
$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

(Continued)

MB90570/A Series

(Continued)



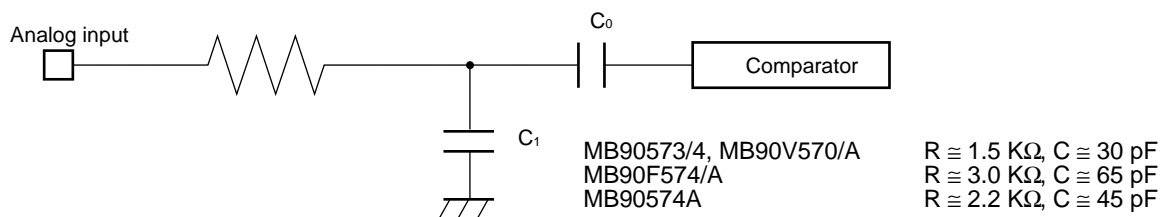
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions. Output impedance values of the external circuit of 7 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @ machine clock of 16 MHz).

• Equipment of analog input circuit model



Note: Listed values must be considered as standards.

• Error

The smaller the $|AVRH - AVRL|$, the greater the error would become relatively.

MB90570/A Series

8. D/A Converter Electrical Characteristics

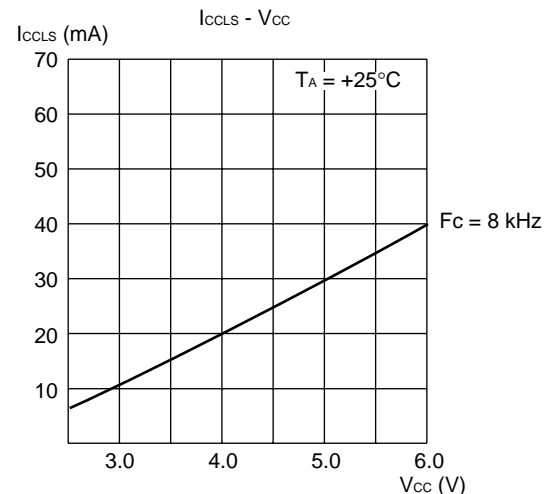
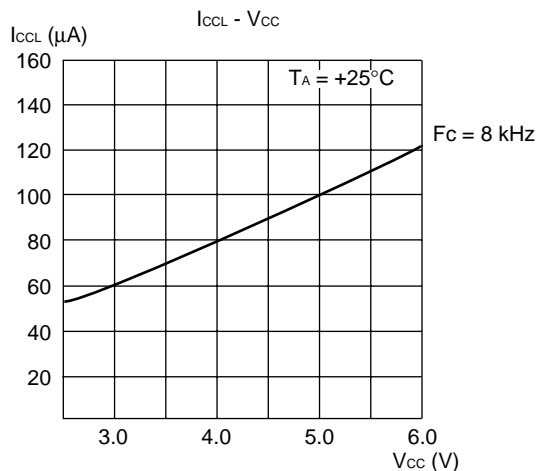
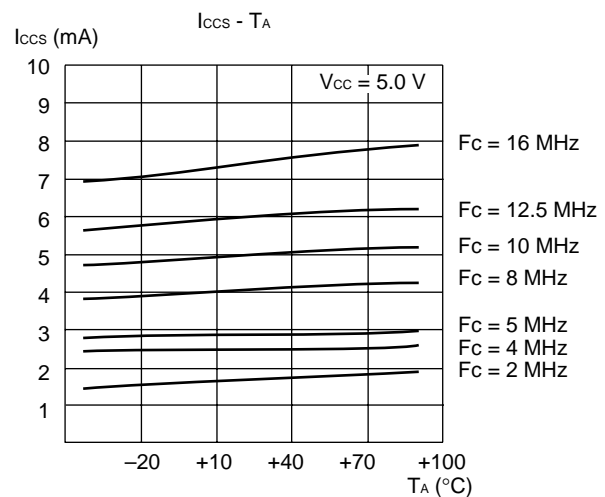
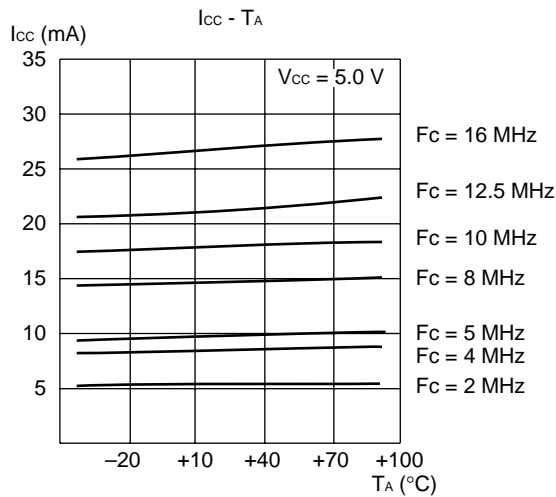
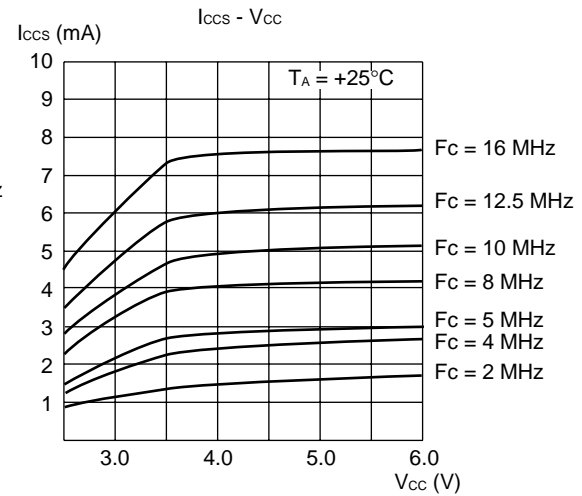
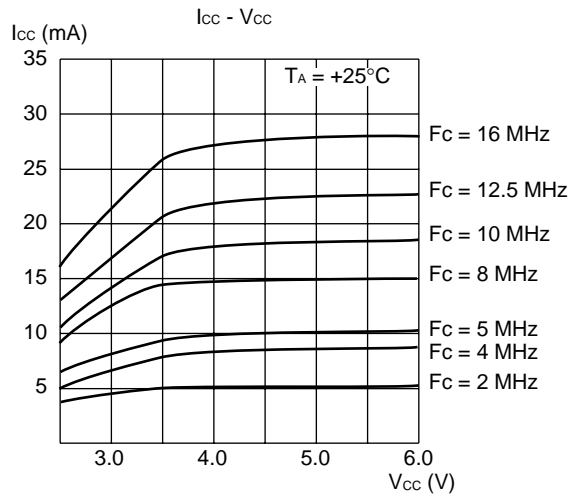
($AV_{CC} = V_{CC} = DV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	8	—	bit	
Differential linearity error	—	—	—	—	± 0.9	LSB	
Absolute accuracy	—	—	—	—	± 1.2	%	
Linearity error	—	—	—	—	± 1.5	LSB	
Conversion time	—	—	—	10	20	μs	Load capacitance: 20 pF
Analog reference voltage	—	DV_{CC}	$V_{SS} + 3.0$	—	AV_{CC}	V	
Reference voltage supply current	I_{DVR}	DV_{CC}	—	120	300	μA	Conversion under no load
	I_{DVRS}	DV_{CC}	—	—	10	μA	In sleep mode
Analog output impedance	—	—	—	20	—	$\text{k}\Omega$	

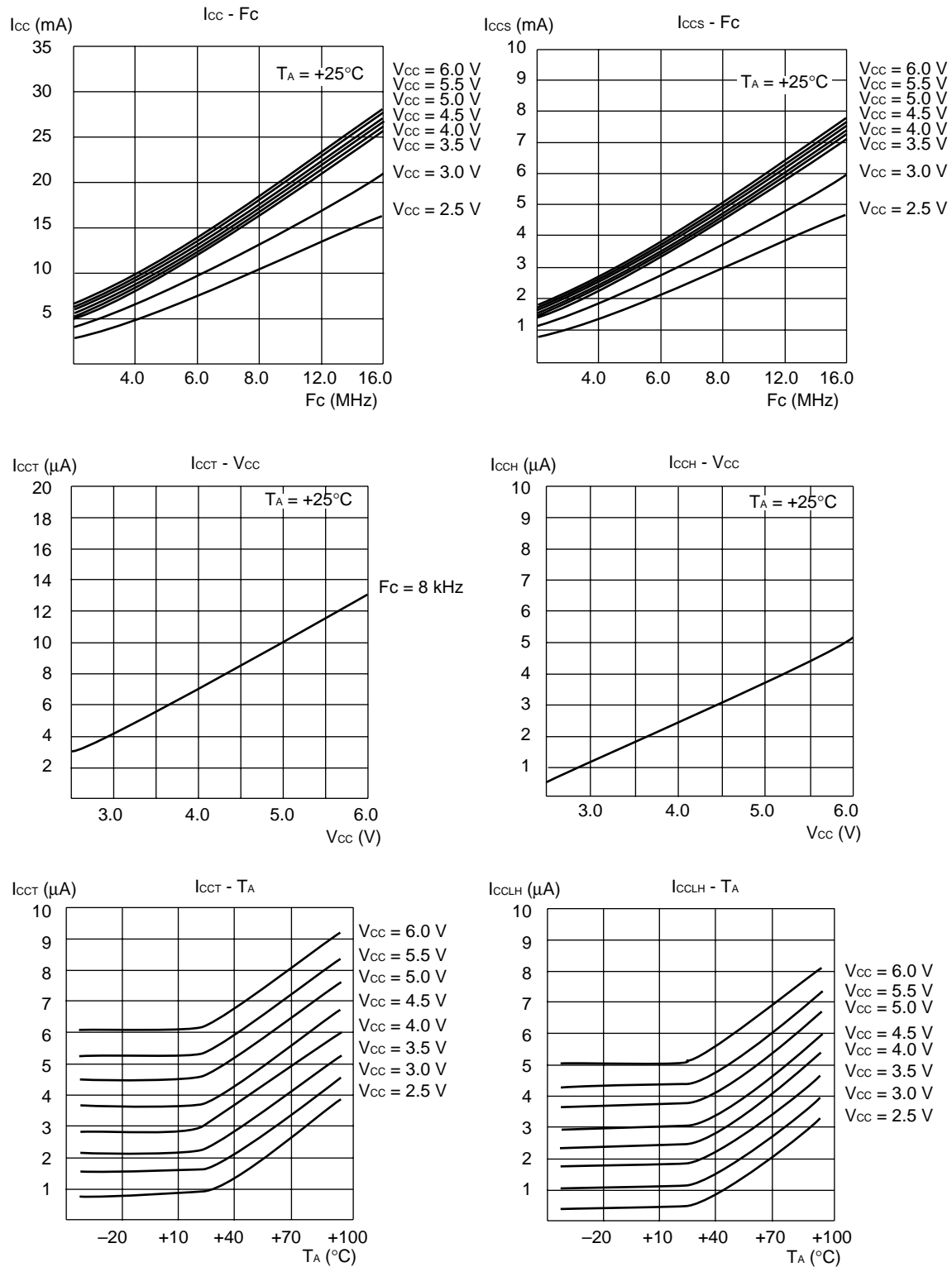
MB90570/A Series

■ EXAMPLE CHARACTERISTICS

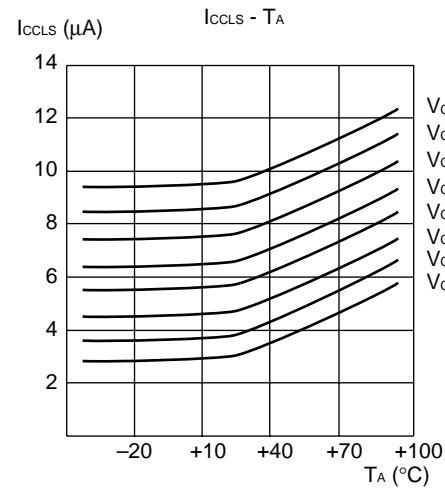
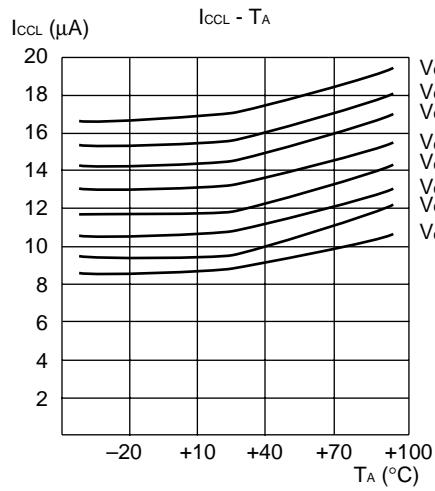
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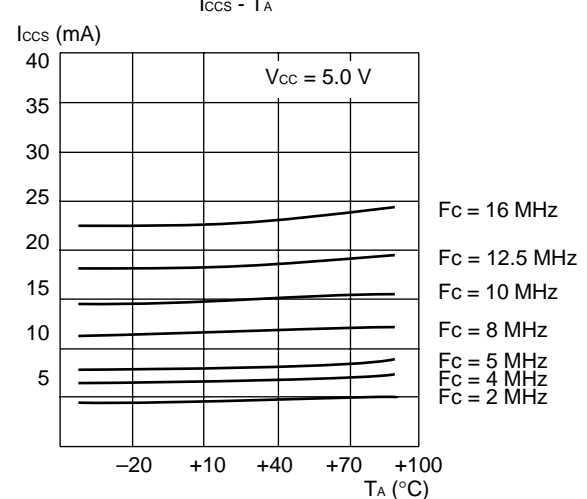
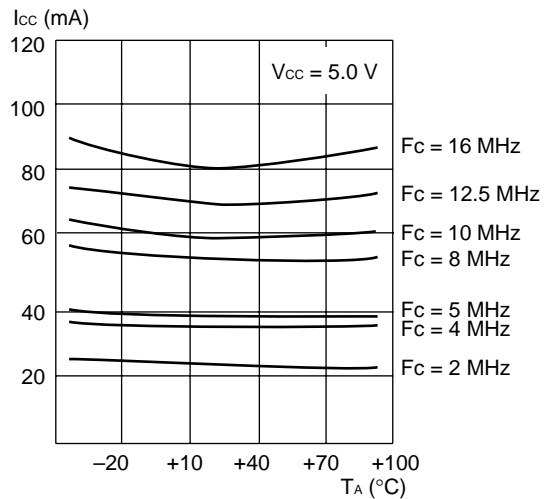
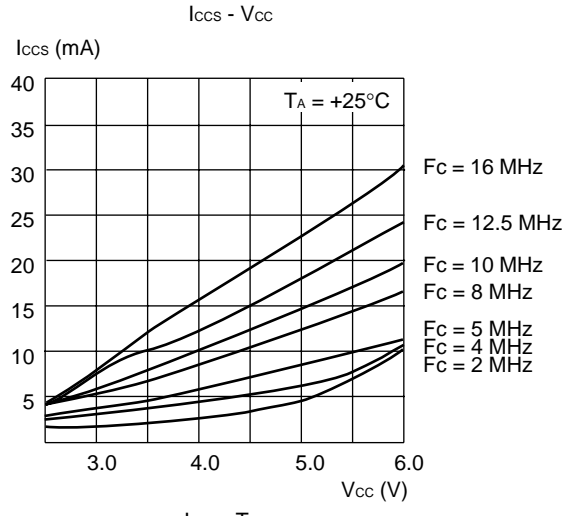
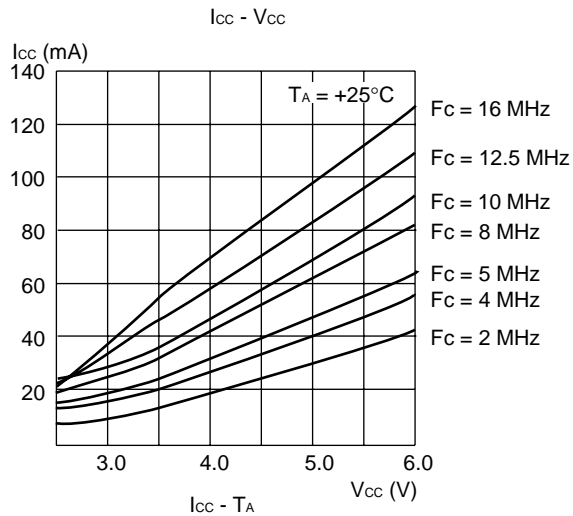
MB90570/A Series



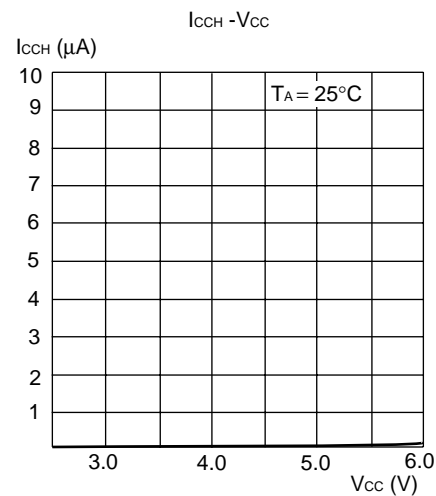
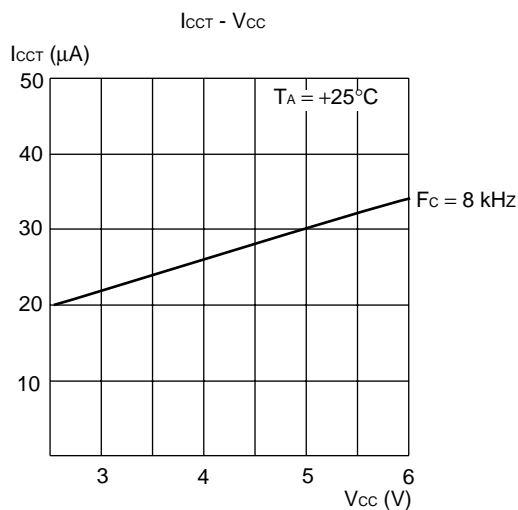
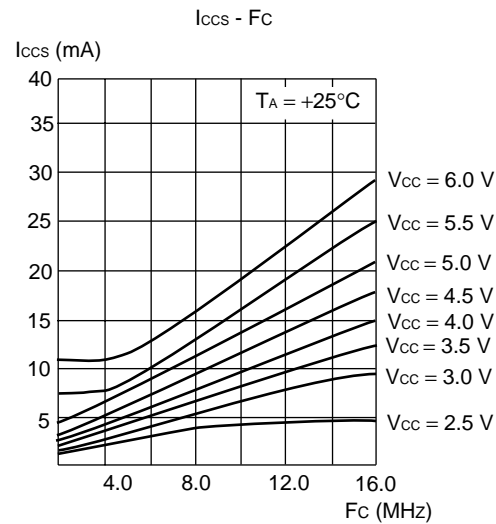
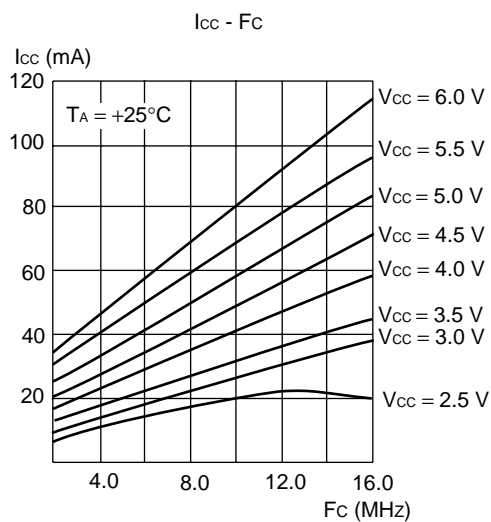
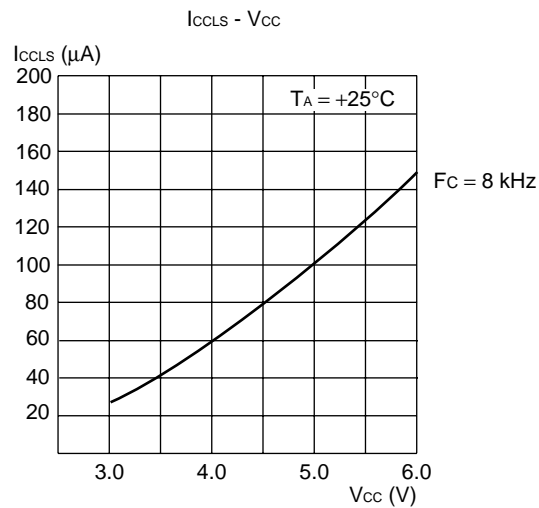
MB90570/A Series



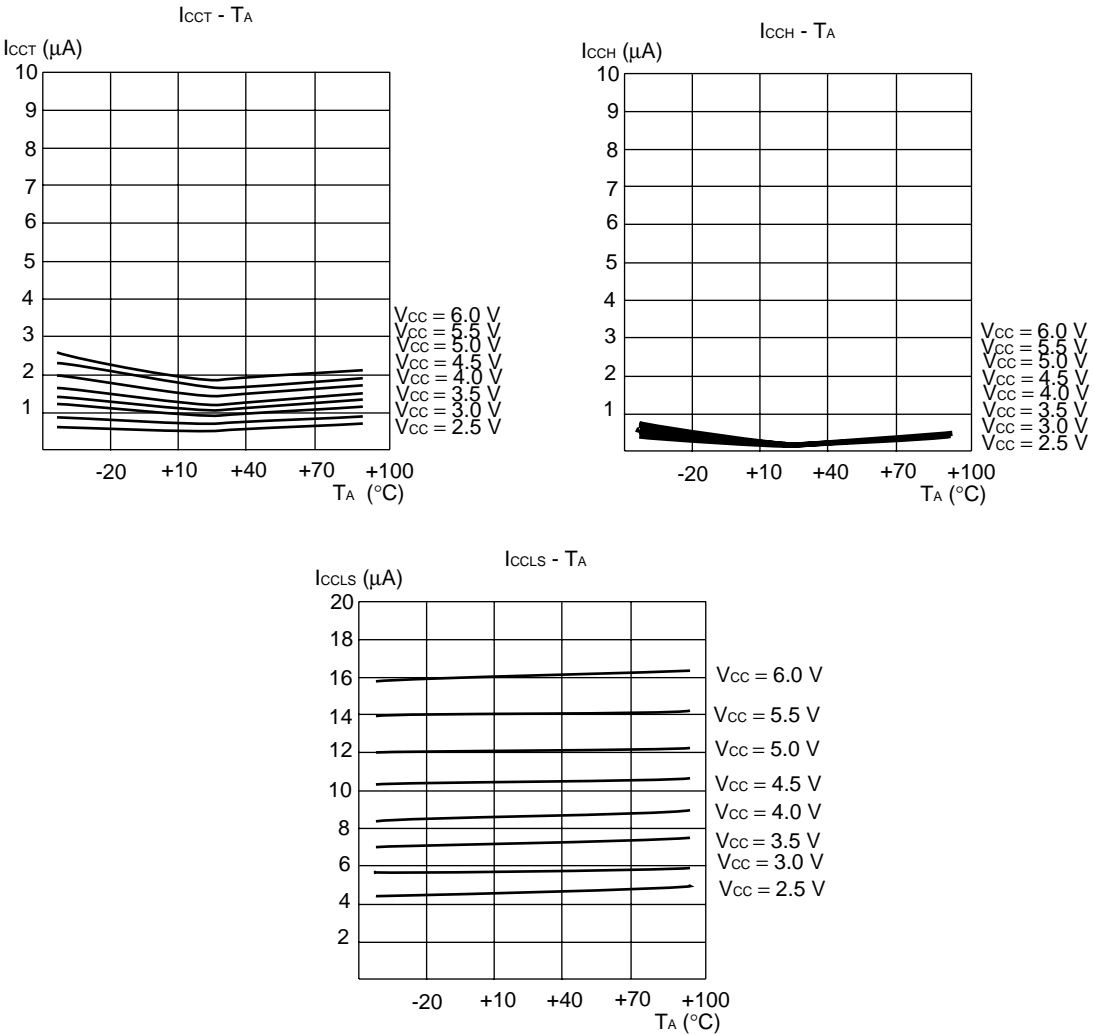
(2) Power Supply Current (MB90F574)



MB90570/A Series

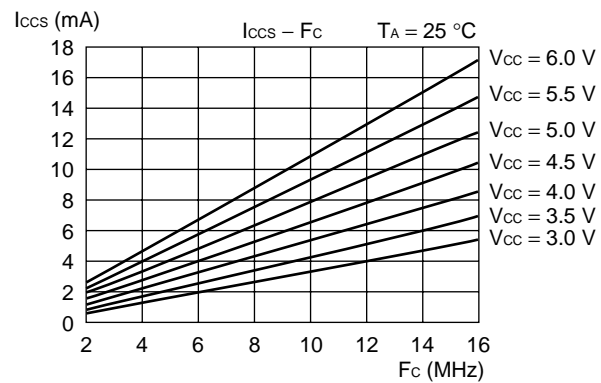
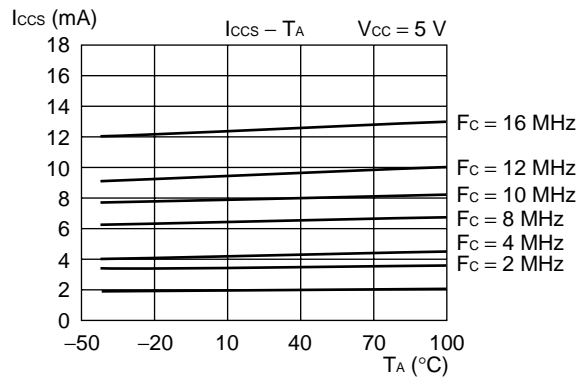
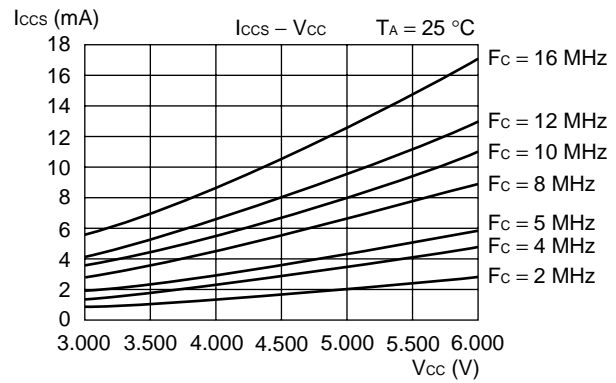
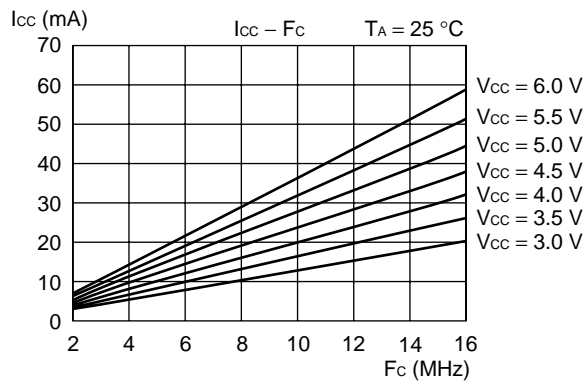
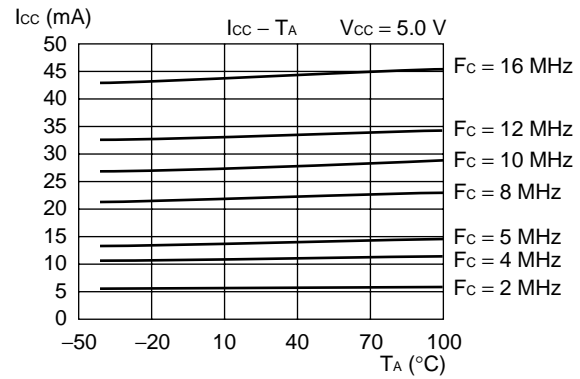
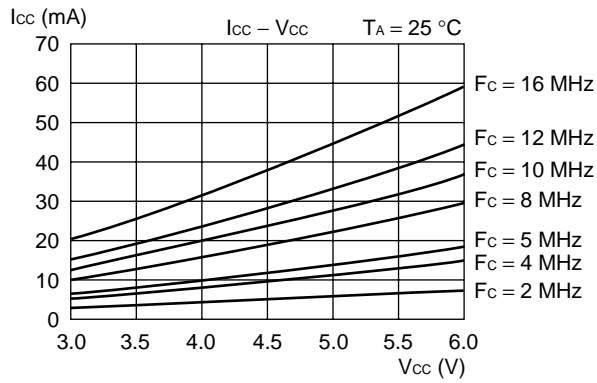


MB90570/A Series

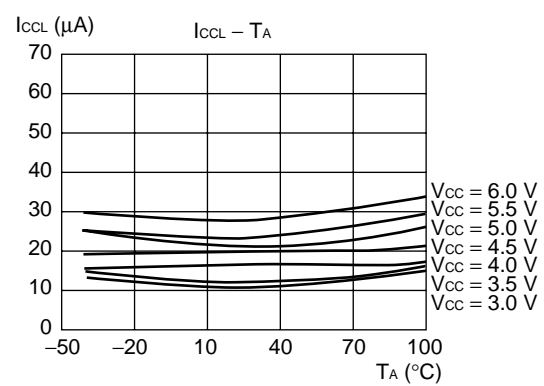
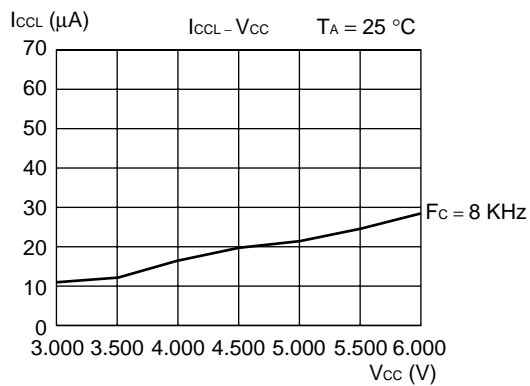
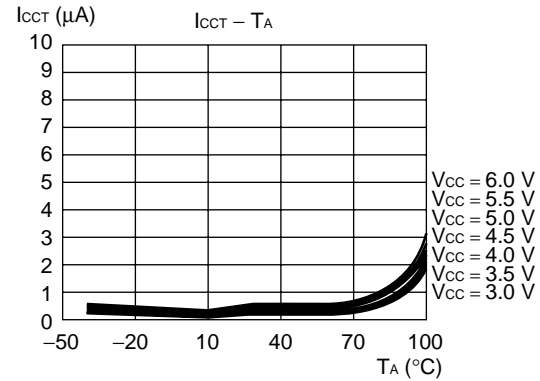
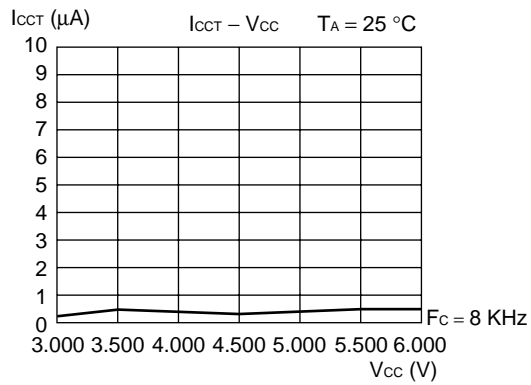
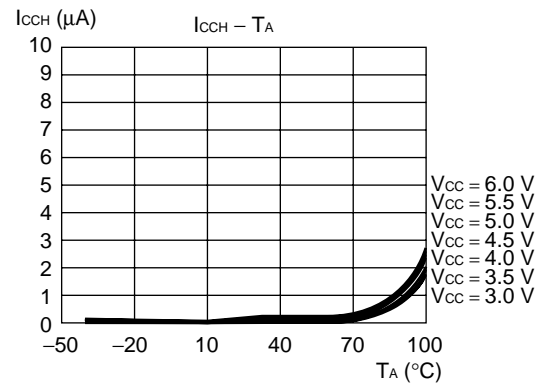
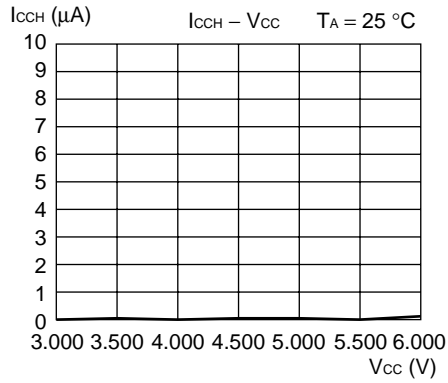


MB90570/A Series

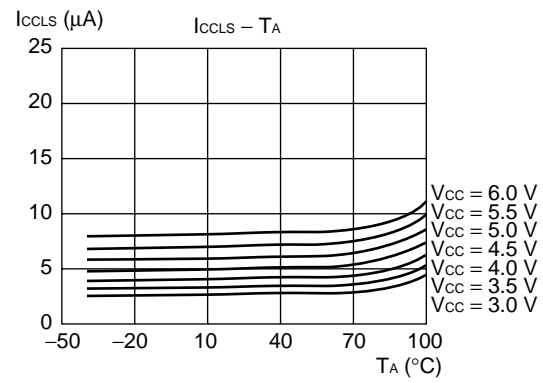
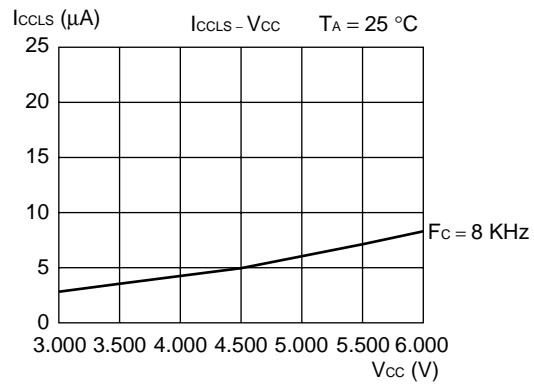
(3)Power Supply Current (MB90574A)



MB90570/A Series



MB90570/A Series



MB90570/A Series

■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction code.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00 _H to AH. X : Transfers 00 _H or FF _H to AH by signing and extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

• Number of execution cycles

The number of cycles required for instruction execution is acquired by adding the number of cycles for each instruction, a corrective value depending on the condition, and the number of cycles required for program fetch. Whenever the instruction being executed exceeds the two-byte (word) boundary, a program on an internal ROM connected to a 16-bit bus is fetched. If data access is interfered with, therefore, the number of execution cycles is increased.

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For each byte of the instruction being executed, a program on a memory connected to an 8-bit external data bus is fetched. If data access is interfered with, therefore, the number of execution cycles is increased. When a general-purpose register, an internal ROM, an internal RAM, an internal I/O device, or an external bus is accessed during intermittent CPU operation, the CPU clock is suspended by the number of cycles specified by the CG1/0 bit of the low-power consumption mode control register. When determining the number of cycles required for instruction execution during intermittent CPU operation, therefore, add the value of the number of times access is done \times the number of cycles suspended as the corrective value to the number of ordinary execution cycles.

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Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL and AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000 _H to 0000FF _H)
#imm4 #imm8 #imm16 #imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
()b	Bit address
rel	PC relative addressing
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

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Table 3 Effective Address Fields

Code	Notation			Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 R1 R2 R3 R4 R5 R6 R7	RW0 RW1 RW2 RW3 RW4 RW5 RW6 RW7	RL0 (RL0) RL1 (RL1) RL2 (RL2) RL3 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3			Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +			Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8			Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16			Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16			Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

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Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a)	Number of register accesses for each type of addressing
		Number of execution cycles for each type of addressing	
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C	@RW0 + RW7	4	2
1D	@RW1 + RW7	4	2
1E	@PC + disp16	2	0
1F	addr16	1	0

Note: “(a)” is used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Compensation Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Cycles	Access	Cycles	Access	Cycles	Access
Internal register	+0	1	+0	1	+0	2
Internal memory even address	+0	1	+0	1	+0	2
Internal memory odd address	+0	1	+2	2	+4	4
Even address on external data bus (16 bits)	+1	1	+1	1	+2	2
Odd address on external data bus (16 bits)	+1	1	+4	2	+8	4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes: • “(b)”, “(c)”, and “(d)” are used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

- When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes: • When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

- Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for “worst case” calculations.

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Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	—	—	—	*	*	—	—	—
MOV A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	—	—	—	*	*	—	—	—
MOV A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	—	—	—	*	*	—	—	—
MOV A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	—	—	—	*	*	—	—	—
MOV A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	—	—	—	*	*	—	—	—
MOV A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	—	—	—	*	*	—	—	—
MOV A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	—	—	—	*	*	—	—	—
MOV A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	—	—	—	—	*	*	—	—	—
MOV A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	Z	*	—	—	—	*	*	—	—	—
MOVN A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	—	—	—	R	*	—	—	—
MOVX A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	—	—	—	*	*	—	—	—
MOVX A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	—	—	—	*	*	—	—	—
MOVX A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	—	—	—	*	*	—	—	—
MOVX A, ear	2	2	1	0	byte (A) ← (ear)	X	*	—	—	—	*	*	—	—	—
MOVX A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	—	—	—	*	*	—	—	—
MOVX A, io	2	3	0	(b)	byte (A) ← (io)	X	*	—	—	—	*	*	—	—	—
MOVX A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	—	—	—	*	*	—	—	—
MOVX A, @A	2	3	0	(b)	byte (A) ← ((A))	X	—	—	—	—	*	*	—	—	—
MOVX A, @RWi+disp8	2	5	1	(b)	byte (A) ← ((RWi)+disp8)	X	*	—	—	—	*	*	—	—	—
MOVX A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	X	*	—	—	—	*	*	—	—	—
MOV dir, A	2	3	0	(b)	byte (dir) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV addr16, A	3	4	0	(b)	byte (addr16) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV Ri, A	1	2	1	0	byte (Ri) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV ear, A	2	2	1	0	byte (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV eam, A	2+	3+ (a)	0	(b)	byte (eam) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV io, A	2	3	0	(b)	byte (io) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV @RLi+disp8, A	3	10	2	(b)	byte ((RLi)+disp8) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV Ri, ear	2	3	2	0	byte (Ri) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOV Ri, eam	2+	4+ (a)	1	(b)	byte (Ri) ← (eam)	—	—	—	—	—	*	*	—	—	—
MOV ear, Ri	2	4	2	0	byte (ear) ← (Ri)	—	—	—	—	—	*	*	—	—	—
MOV eam, Ri	2+	5+ (a)	1	(b)	byte (eam) ← (Ri)	—	—	—	—	—	*	*	—	—	—
MOV Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	—	—	—	—	—	*	*	—	—	—
MOV io, #imm8	3	5	0	(b)	byte (io) ← imm8	—	—	—	—	—	—	—	—	—	—
MOV dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	—	—	—	—	—	—	—	—	—	—
MOV ear, #imm8	3	2	1	0	byte (ear) ← imm8	—	—	—	—	—	*	*	—	—	—
MOV eam, #imm8	3+	4+ (a)	0	(b)	byte (eam) ← imm8	—	—	—	—	—	—	—	—	—	—
MOV @AL, AH															
/MOV @A, T	2	3	0	(b)	byte ((A)) ← (AH)	—	—	—	—	—	*	*	—	—	—
XCH A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	—	—	—	—	—	—	—	—	—
XCH A, eam	2+	5+ (a)	0	2× (b)	byte (A) ↔ (eam)	Z	—	—	—	—	—	—	—	—	—
XCH Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	—	—	—	—	—	—	—	—	—	—
XCH Ri, eam	2+	9+ (a)	2	2× (b)	byte (Ri) ↔ (eam)	—	—	—	—	—	—	—	—	—	—

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	—	*	—	—	—	*	*	—	—	—
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	—	*	—	—	—	*	*	—	—	—
MOVW A, SP	1	1	0	0	word (A) ← (SP)	—	*	—	—	—	*	*	—	—	—
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	—	*	—	—	—	*	*	—	—	—
MOVW A, ear	2	2	1	0	word (A) ← (ear)	—	*	—	—	—	*	*	—	—	—
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	—	*	—	—	—	*	*	—	—	—
MOVW A, io	2	3	0	(c)	word (A) ← (io)	—	*	—	—	—	*	*	—	—	—
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	—	—	—	—	—	*	*	—	—	—
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	—	*	—	—	—	*	*	—	—	—
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	—	*	—	—	—	*	*	—	—	—
MOVW A, @RLi+disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	—	*	—	—	—	*	*	—	—	—
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW SP, A	1	1	0	0	word (SP) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW ear, A	2	2	1	0	word (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW eam, A	2+	3+ (a)	0	(c)	word (eam) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW io, A	2	3	0	(c)	word (io) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW @RWi+disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW @RLi+disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, ear	2	3	2	(0)	word (RWi) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, eam	2+	4+ (a)	1	(c)	word (RWi) ← (eam)	—	—	—	—	—	*	*	—	—	—
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	—	—	—	—	—	*	*	—	—	—
MOVW eam, RWi	2+	5+ (a)	1	(c)	word (eam) ← (RWi)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	—	—	—	—	—	*	*	—	—	—
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	—	—	—	—	—	—	—	—	—	—
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	—	—	—	—	—	*	*	—	—	—
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← imm16	—	—	—	—	—	—	—	—	—	—
MOVW @AL, AH /MOVW @A, T	2	3	0	(c)	word ((A)) ← (AH)	—	—	—	—	—	*	*	—	—	—
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	—	—	—	—	—	—	—	—	—	—
XCHW A, eam	2+	5+ (a)	0	2× (c)	word (A) ↔ (eam)	—	—	—	—	—	—	—	—	—	—
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	—	—	—	—	—	—	—	—	—	—
XCHW RWi, eam	2+	9+ (a)	2	2× (c)	word (RWi) ↔ (eam)	—	—	—	—	—	—	—	—	—	—
MOVL A, ear	2	4	2	0	long (A) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	—	—	—	—	—	*	*	—	—	—
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	—	—	—	—	—	*	*	—	—	—
MOVL ear, A	2	4	2	0	long (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	—	—	—	—	—	*	*	—	—	—

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD A, #imm8	2	2	0	0	byte (A) \leftarrow (A) +imm8	Z	—	—	—	—	*	*	*	*	—
ADD A, dir	2	5	0	(b)	byte (A) \leftarrow (A) +(dir)	Z	—	—	—	—	*	*	*	*	—
ADD A, ear	2	3	1	0	byte (A) \leftarrow (A) +(ear)	Z	—	—	—	—	*	*	*	*	—
ADD A, eam	2+	4+ (a)	0	(b)	byte (A) \leftarrow (A) +(eam)	Z	—	—	—	—	*	*	*	*	—
ADD ear, A	2	3	2	0	byte (ear) \leftarrow (ear) + (A)	—	—	—	—	—	*	*	*	*	—
ADD eam, A	2+	5+ (a)	0	2× (b)	byte (eam) \leftarrow (eam) + (A)	Z	—	—	—	—	*	*	*	*	*
ADDC A	1	2	0	0	byte (A) \leftarrow (AH) + (AL) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDC A, ear	2	3	1	0	byte (A) \leftarrow (A) + (ear) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDC A, eam	2+	4+ (a)	0	(b)	byte (A) \leftarrow (A) + (eam) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDDC A	1	3	0	0	byte (A) \leftarrow (AH) + (AL) + (C) (decimal)	Z	—	—	—	—	*	*	*	*	—
SUB A, #imm8	2	2	0	0	byte (A) \leftarrow (A) -imm8	Z	—	—	—	—	*	*	*	*	—
SUB A, dir	2	5	0	(b)	byte (A) \leftarrow (A) - (dir)	Z	—	—	—	—	*	*	*	*	—
SUB A, ear	2	3	1	0	byte (A) \leftarrow (A) - (ear)	Z	—	—	—	—	*	*	*	*	—
SUB A, eam	2+	4+ (a)	0	(b)	byte (A) \leftarrow (A) - (eam)	Z	—	—	—	—	*	*	*	*	—
SUB ear, A	2	3	2	0	byte (ear) \leftarrow (ear) - (A)	—	—	—	—	—	*	*	*	*	—
SUB eam, A	2+	5+ (a)	0	2× (b)	byte (eam) \leftarrow (eam) - (A)	—	—	—	—	—	*	*	*	*	*
SUBC A	1	2	0	0	byte (A) \leftarrow (AH) - (AL) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBC A, ear	2	3	1	0	byte (A) \leftarrow (A) - (ear) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBC A, eam	2+	4+ (a)	0	(b)	byte (A) \leftarrow (A) - (eam) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBDC A	1	3	0	0	byte (A) \leftarrow (AH) - (AL) - (C) (decimal)	Z	—	—	—	—	*	*	*	*	—
ADDW A	1	2	0	0	word (A) \leftarrow (AH) + (AL)	—	—	—	—	—	*	*	*	*	—
ADDW A, ear	2	3	1	0	word (A) \leftarrow (A) +(ear)	—	—	—	—	—	*	*	*	*	—
ADDW A, eam	2+	4+ (a)	0	(c)	word (A) \leftarrow (A) +(eam)	—	—	—	—	—	*	*	*	*	—
ADDW A, #imm16	3	2	0	0	word (A) \leftarrow (A) +imm16	—	—	—	—	—	*	*	*	*	—
ADDW ear, A	2	3	2	0	word (ear) \leftarrow (ear) + (A)	—	—	—	—	—	*	*	*	*	—
ADDW eam, A	2+	5+ (a)	0	2× (c)	word (eam) \leftarrow (eam) + (A)	—	—	—	—	—	*	*	*	*	*
ADDCW A, ear	2	3	1	0	word (A) \leftarrow (A) + (ear) + (C)	—	—	—	—	—	*	*	*	*	—
ADDCW A, eam	2+	4+ (a)	0	(c)	word (A) \leftarrow (A) + (eam) + (C)	—	—	—	—	—	*	*	*	*	—
SUBW A	1	2	0	0	word (A) \leftarrow (AH) - (AL)	—	—	—	—	—	*	*	*	*	—
SUBW A, ear	2	3	1	0	word (A) \leftarrow (A) - (ear)	—	—	—	—	—	*	*	*	*	—
SUBW A, eam	2+	4+ (a)	0	(c)	word (A) \leftarrow (A) - (eam)	—	—	—	—	—	*	*	*	*	—
SUBW A, #imm16	3	2	0	0	word (A) \leftarrow (A) -imm16	—	—	—	—	—	*	*	*	*	—
SUBW ear, A	2	3	2	0	word (ear) \leftarrow (ear) - (A)	—	—	—	—	—	*	*	*	*	—
SUBW eam, A	2+	5+ (a)	0	2× (c)	word (eam) \leftarrow (eam) - (A)	—	—	—	—	—	*	*	*	*	*
SUBCW A, ear	2	3	1	0	word (A) \leftarrow (A) - (ear) - (C)	—	—	—	—	—	*	*	*	*	—
SUBCW A, eam	2+	4+ (a)	0	(c)	word (A) \leftarrow (A) - (eam) - (C)	—	—	—	—	—	*	*	*	*	—
ADDL A, ear	2	6	2	0	long (A) \leftarrow (A) + (ear)	—	—	—	—	—	*	*	*	*	—
ADDL A, eam	2+	7+ (a)	0	(d)	long (A) \leftarrow (A) + (eam)	—	—	—	—	—	*	*	*	*	—
ADDL A, #imm32	5	4	0	0	long (A) \leftarrow (A) +imm32	—	—	—	—	—	*	*	*	*	—
SUBL A, ear	2	6	2	0	long (A) \leftarrow (A) - (ear)	—	—	—	—	—	*	*	*	*	—
SUBL A, eam	2+	7+ (a)	0	(d)	long (A) \leftarrow (A) - (eam)	—	—	—	—	—	*	*	*	*	—
SUBL A, #imm32	5	4	0	0	long (A) \leftarrow (A) -imm32	—	—	—	—	—	*	*	*	*	—

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC ear	2	2	2	0	byte (ear) \leftarrow (ear) +1	—	—	—	—	—	*	*	*	—	—
INC eam	2+	5+ (a)	0	2× (b)	byte (eam) \leftarrow (eam) +1	—	—	—	—	—	*	*	*	—	*
DEC ear	2	3	2	0	byte (ear) \leftarrow (ear) –1	—	—	—	—	—	*	*	*	—	—
DEC eam	2+	5+ (a)	0	2× (b)	byte (eam) \leftarrow (eam) –1	—	—	—	—	—	*	*	*	—	*
INCW ear	2	3	2	0	word (ear) \leftarrow (ear) +1	—	—	—	—	—	*	*	*	—	—
INCW eam	2+	5+ (a)	0	2× (c)	word (eam) \leftarrow (eam) +1	—	—	—	—	—	*	*	*	—	*
DECW ear	2	3	2	0	word (ear) \leftarrow (ear) –1	—	—	—	—	—	*	*	*	—	—
DECW eam	2+	5+ (a)	0	2× (c)	word (eam) \leftarrow (eam) –1	—	—	—	—	—	*	*	*	—	*
INCL ear	2	7	4	0	long (ear) \leftarrow (ear) +1	—	—	—	—	—	*	*	*	—	—
INCL eam	2+	9+ (a)	0	2× (d)	long (eam) \leftarrow (eam) +1	—	—	—	—	—	*	*	*	—	*
DECL ear	2	7	4	0	long (ear) \leftarrow (ear) –1	—	—	—	—	—	*	*	*	—	—
DECL eam	2+	9+ (a)	0	2× (d)	long (eam) \leftarrow (eam) –1	—	—	—	—	—	*	*	*	—	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP A	1	1	0	0	byte (AH) – (AL)	—	—	—	—	—	*	*	*	*	—
CMP A, ear	2	2	1	0	byte (A) \leftarrow (ear)	—	—	—	—	—	*	*	*	*	—
CMP A, eam	2+	3+ (a)	0	(b)	byte (A) \leftarrow (eam)	—	—	—	—	—	*	*	*	*	—
CMP A, #imm8	2	2	0	0	byte (A) \leftarrow imm8	—	—	—	—	—	*	*	*	*	—
CMPW A	1	1	0	0	word (AH) – (AL)	—	—	—	—	—	*	*	*	*	—
CMPW A, ear	2	2	1	0	word (A) \leftarrow (ear)	—	—	—	—	—	*	*	*	*	—
CMPW A, eam	2+	3+ (a)	0	(c)	word (A) \leftarrow (eam)	—	—	—	—	—	*	*	*	*	—
CMPW A, #imm16	3	2	0	0	word (A) \leftarrow imm16	—	—	—	—	—	*	*	*	*	—
CMPL A, ear	2	6	2	0	word (A) \leftarrow (ear)	—	—	—	—	—	*	*	*	*	—
CMPL A, eam	2+	7+ (a)	0	(d)	word (A) \leftarrow (eam)	—	—	—	—	—	*	*	*	*	—
CMPL A, #imm32	5	3	0	0	word (A) \leftarrow imm32	—	—	—	—	—	*	*	*	*	—

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	—	—	—	—	—	—	—	*	*	—
DIVU A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	—	—	—	—	—	—	—	*	*	—
DIVU A, eam	2+	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	—	—	—	—	—	—	—	*	*	—
DIVUW A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	—	—	—	—	—	—	—	*	*	—
DIVUW A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (ear)	—	—	—	—	—	—	—	*	*	—
MULU A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	—	—	—	—	—	—	—	—	—	—
MULU A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	—	—	—	—	—	—	—	—	—	—
MULU A, eam	2+	*10	0	(b)	byte (A) *byte (eam) → word (A)	—	—	—	—	—	—	—	—	—	—
MULUW A	1	*11	0	0	word (AH) *word (AL) → long (A)	—	—	—	—	—	—	—	—	—	—
MULUW A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	—	—	—	—	—	—	—	—	—	—
MULUW A, eam	2+	*13	0	(c)	word (A) *word (eam) → long (A)	—	—	—	—	—	—	—	—	—	—

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.

*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.

*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.

*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.

*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.

*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.

*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.

*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.

*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.

*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.

*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.

*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.

*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 13 Signed Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIV A	2	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	Z	—	—	—	—	—	—	*	*	—
DIV A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	Z	—	—	—	—	—	—	*	*	—
DIV A, eam	2 +	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	Z	—	—	—	—	—	—	*	*	—
DIVW A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	—	—	—	—	—	—	—	*	*	—
DIVW A, eam	2 +	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	—	—	—	—	—	—	—	*	*	—
MULU A	2	*8	0	0	byte (AH) *byte (AL) → word (A)	—	—	—	—	—	—	—	—	—	—
MULU A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	—	—	—	—	—	—	—	—	—	—
MULU A, eam	2 +	*10	0	(b)	byte (A) *byte (eam) → word (A)	—	—	—	—	—	—	—	—	—	—
MULUW A	2	*11	0	0	word (AH) *word (AL) → long (A)	—	—	—	—	—	—	—	—	—	—
MULUW A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	—	—	—	—	—	—	—	—	—	—
MULUW A, eam	2 +	*13	0	(c)	word (A) *word (eam) → long (A)	—	—	—	—	—	—	—	—	—	—

*1: Set to 3 when the division-by-0, 8 or 18 for an overflow, and 18 for normal operation.

*2: Set to 3 when the division-by-0, 10 or 21 for an overflow, and 22 for normal operation.

*3: Set to 4 + (a) when the division-by-0, 11 + (a) or 22 + (a) for an overflow, and 23 + (a) for normal operation.

*4: Positive dividend: Set to 4 when the division-by-0, 10 or 29 for an overflow, and 30 for normal operation.

Negative dividend: Set to 4 when the division-by-0, 11 or 30 for an overflow and 31 for normal operation.

*5: Positive dividend: Set to 4 + (a) when the division-by-0, 11 + (a) or 30 + (a) for an overflow, and 31 + (a) for normal operation.

Negative dividend: Set to 4 + (a) when the division-by-0, 12 + (a) or 31 + (a) for an overflow, and 32 + (a) for normal operation.

*6: When the division-by-0, (b) for an overflow, and $2 \times (b)$ for normal operation.

*7: When the division-by-0, (c) for an overflow, and $2 \times (c)$ for normal operation.

*8: Set to 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*9: Set to 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.

*10: Set to 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.

*11: Set to 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*12: Set to 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.

*13: Set to 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Notes: • When overflow occurs during DIV or DIVW instruction execution, the number of execution cycles takes two values because of detection before and after an operation.

• When overflow occurs during DIV or DIVW instruction execution, the contents of AL are destroyed.

• For (a) to (d), refer to "Table 4 Number of Execution Cycles for Effective Address in Addressing Modes" and "Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles."

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Table 14 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	—	—	—	—	—	*	*	R	—	—
AND A, ear	2	3	1	0	byte (A) ← (A) and (ear)	—	—	—	—	—	*	*	R	—	—
AND A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	—	—	—	—	—	*	*	R	—	—
AND ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	—	—	—	—	—	*	*	R	—	—
AND eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	—	—	—	—	—	*	*	R	—	*
OR A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	—	—	—	—	—	*	*	R	—	—
OR A, ear	2	3	1	0	byte (A) ← (A) or (ear)	—	—	—	—	—	*	*	R	—	—
OR A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	—	—	—	—	—	*	*	R	—	—
OR ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	—	—	—	—	—	*	*	R	—	—
OR eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	—	—	—	—	—	*	*	R	—	*
XOR A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	—	—	—	—	—	*	*	R	—	—
XOR A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	—	—	—	—	—	*	*	R	—	—
XOR A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	—	—	—	—	—	*	*	R	—	—
XOR ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	—	—	—	—	—	*	*	R	—	—
XOR eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	—	—	—	—	—	*	*	R	—	*
NOT A	1	2	0	0	byte (A) ← not (A)	—	—	—	—	—	*	*	R	—	—
NOT ear	2	3	2	0	byte (ear) ← not (ear)	—	—	—	—	—	*	*	R	—	—
NOT eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	—	—	—	—	—	*	*	R	—	*
ANDW A	1	2	0	0	word (A) ← (AH) and (A)	—	—	—	—	—	*	*	R	—	—
ANDW A, #imm16	3	2	0	0	word (A) ← (A) and imm16	—	—	—	—	—	*	*	R	—	—
ANDW A, ear	2	3	1	0	word (A) ← (A) and (ear)	—	—	—	—	—	*	*	R	—	—
ANDW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	—	—	—	—	—	*	*	R	—	—
ANDW ear, A	2	3	2	0	word (ear) ← (ear) and (A)	—	—	—	—	—	*	*	R	—	—
ANDW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	—	—	—	—	—	*	*	R	—	*
ORW A	1	2	0	0	word (A) ← (AH) or (A)	—	—	—	—	—	*	*	R	—	—
ORW A, #imm16	3	2	0	0	word (A) ← (A) or imm16	—	—	—	—	—	*	*	R	—	—
ORW A, ear	2	3	1	0	word (A) ← (A) or (ear)	—	—	—	—	—	*	*	R	—	—
ORW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	—	—	—	—	—	*	*	R	—	—
ORW ear, A	2	3	2	0	word (ear) ← (ear) or (A)	—	—	—	—	—	*	*	R	—	—
ORW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	—	—	—	—	—	*	*	R	—	*
XORW A	1	2	0	0	word (A) ← (AH) xor (A)	—	—	—	—	—	*	*	R	—	—
XORW A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	—	—	—	—	—	*	*	R	—	—
XORW A, ear	2	3	1	0	word (A) ← (A) xor (ear)	—	—	—	—	—	*	*	R	—	—
XORW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	—	—	—	—	—	*	*	R	—	—
XORW ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	—	—	—	—	—	*	*	R	—	—
XORW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	—	—	—	—	—	*	*	R	—	*
NOTW A	1	2	0	0	word (A) ← not (A)	—	—	—	—	—	*	*	R	—	—
NOTW ear	2	3	2	0	word (ear) ← not (ear)	—	—	—	—	—	*	*	R	—	—
NOTW eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	—	—	—	—	—	*	*	R	—	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) \leftarrow (A) and (ear)	—	—	—	—	—	*	*	R	—	—
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) \leftarrow (A) and (eam)	—	—	—	—	—	*	*	R	—	—
ORL A, ear	2	6	2	0	long (A) \leftarrow (A) or (ear)	—	—	—	—	—	*	*	R	—	—
ORL A, eam	2+	7+ (a)	0	(d)	long (A) \leftarrow (A) or (eam)	—	—	—	—	—	*	*	R	—	—
XORL A, ea	2	6	2	0	long (A) \leftarrow (A) xor (ear)	—	—	—	—	—	*	*	R	—	—
XORL A, eam	2+	7+ (a)	0	(d)	long (A) \leftarrow (A) xor (eam)	—	—	—	—	—	*	*	R	—	—

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) \leftarrow 0 – (A)	X	—	—	—	—	*	*	*	*	—
NEG ear	2	3	2	0	byte (ear) \leftarrow 0 – (ear)	—	—	—	—	—	*	*	*	*	—
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) \leftarrow 0 – (eam)	—	—	—	—	—	*	*	*	*	*
NEGW A	1	2	0	0	word (A) \leftarrow 0 – (A)	—	—	—	—	—	*	*	*	*	—
NEGW ear	2	3	2	0	word (ear) \leftarrow 0 – (ear)	—	—	—	—	—	*	*	*	*	—
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) \leftarrow 0 – (eam)	—	—	—	—	—	*	*	*	*	*

Table 17 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) \leftarrow Shift until first digit is “1” byte (R0) \leftarrow Current shift count	—	—	—	—	—	—	*	—	—	—

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 18 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← Right rotation with carry	—	—	—	—	—	*	*	—	*	—
ROLC A	2	2	0	0	byte (A) ← Left rotation with carry	—	—	—	—	—	*	*	—	*	—
RORC ear	2	3	2	0	byte (ear) ← Right rotation with carry	—	—	—	—	—	*	*	—	*	—
RORC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Right rotation with carry	—	—	—	—	—	*	*	—	*	*
ROLC ear	2	3	2	0	byte (ear) ← Left rotation with carry	—	—	—	—	—	*	*	—	*	—
ROLC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Left rotation with carry	—	—	—	—	—	*	*	—	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	—	—	—	—	—	*	*	—	*	—
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	—	—	—	—	*	*	*	—	*	—
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	—	—	—	—	*	R	*	—	*	—
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	—	—	—	—	—	*	*	—	*	—
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSRW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSLW A, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	—	—	—	—	—	*	*	—	*	—
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	—	—	—	—	*	*	*	—	*	—
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	—	—	—	—	—	*	*	—	*	—

*1: 6 when R0 is 0, 5 + (R0) in all other cases.

*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 19 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch when (Z) = 1	—	—	—	—	—	—	—	—	—	—
BNZ/BNE rel	2	*1	0	0	Branch when (Z) = 0	—	—	—	—	—	—	—	—	—	—
BC/BLO rel	2	*1	0	0	Branch when (C) = 1	—	—	—	—	—	—	—	—	—	—
BNC/BHS rel	2	*1	0	0	Branch when (C) = 0	—	—	—	—	—	—	—	—	—	—
BN rel	2	*1	0	0	Branch when (N) = 1	—	—	—	—	—	—	—	—	—	—
BP rel	2	*1	0	0	Branch when (N) = 0	—	—	—	—	—	—	—	—	—	—
BV rel	2	*1	0	0	Branch when (V) = 1	—	—	—	—	—	—	—	—	—	—
BNV rel	2	*1	0	0	Branch when (V) = 0	—	—	—	—	—	—	—	—	—	—
BT rel	2	*1	0	0	Branch when (T) = 1	—	—	—	—	—	—	—	—	—	—
BNT rel	2	*1	0	0	Branch when (T) = 0	—	—	—	—	—	—	—	—	—	—
BLT rel	2	*1	0	0	Branch when (V) xor (N) = 1	—	—	—	—	—	—	—	—	—	—
BGE rel	2	*1	0	0	Branch when (V) xor (N) = 0	—	—	—	—	—	—	—	—	—	—
BLE rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 1	—	—	—	—	—	—	—	—	—	—
BGT rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 0	—	—	—	—	—	—	—	—	—	—
BLS rel	2	*1	0	0	Branch when (C) or (Z) = 1	—	—	—	—	—	—	—	—	—	—
BHI rel	2	*1	0	0	Branch when (C) or (Z) = 0	—	—	—	—	—	—	—	—	—	—
BRA rel	2	*1	0	0	Branch unconditionally	—	—	—	—	—	—	—	—	—	—
JMP @A	1	2	0	0	word (PC) ← (A)	—	—	—	—	—	—	—	—	—	—
JMP addr16	3	3	0	0	word (PC) ← addr16	—	—	—	—	—	—	—	—	—	—
JMP @ear	2	3	1	0	word (PC) ← (ear)	—	—	—	—	—	—	—	—	—	—
JMP @eam	2+	4+ (a)	0	(c)	word (PC) ← (eam)	—	—	—	—	—	—	—	—	—	—
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear +2)	—	—	—	—	—	—	—	—	—	—
JMPP @eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	—	—	—	—	—	—	—	—	—	—
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	—	—	—	—	—	—	—	—	—	—
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	—	—	—	—	—	—	—	—	—	—
CALL @eam *4	2+	7+ (a)	0	2× (c)	word (PC) ← (eam)	—	—	—	—	—	—	—	—	—	—
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	—	—	—	—	—	—	—	—	—	—
CALLV #vct4 *5	1	7	0	2× (c)	Vector call instruction	—	—	—	—	—	—	—	—	—	—
CALLP @ear *6	2	10	2	2× (c)	word (PC) ← (ear) 0 to 15, (PCB) ← (ear) 16 to 23	—	—	—	—	—	—	—	—	—	—
CALLP @eam *6	2+	11+ (a)	0	*2	word (PC) ← (eam) 0 to 15, (PCB) ← (eam) 16 to 23	—	—	—	—	—	—	—	—	—	—
CALLP addr24 *7	4	10	0	2× (c)	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	—	—	—	—	—	—	—	—	—	—

*1: 4 when branching, 3 when not branching.

*2: (b) + 3 × (c)

*3: Read (word) branch address.

*4: W: Save (word) to stack; R: read (word) branch address.

*5: Save (word) to stack.

*6: W: Save (long word) to W stack; R: read (long word) R branch address.

*7: Save (long word) to stack.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 20 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) \neq imm8	—	—	—	—	—	*	*	*	*	—
CWBNE A, #imm16, rel	4	*1	0	0	Branch when word (A) \neq imm16	—	—	—	—	—	*	*	*	*	—
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) \neq imm8	—	—	—	—	—	*	*	*	*	—
CBNE eam, #imm8, rel ^{*10}	4+	*3	0	(b)	Branch when byte (eam) \neq imm8	—	—	—	—	—	*	*	*	*	—
CWBNE ear, #imm16, rel	5	*4	1	0	Branch when word (ear) \neq imm16	—	—	—	—	—	*	*	*	*	—
CWBNE eam, #imm16, rel ^{*10}	5+	*3	0	(c)	Branch when word (eam) \neq imm16	—	—	—	—	—	*	*	*	*	—
DBNZ ear, rel	3	*5	2	0	Branch when byte (ear) = (ear) – 1, and (ear) \neq 0	—	—	—	—	—	*	*	*	—	—
DBNZ eam, rel	3+	*6	2	2× (b)	Branch when byte (eam) = (eam) – 1, and (eam) \neq 0	—	—	—	—	—	*	*	*	—	*
DWBNZ ear, rel	3	*5	2	0	Branch when word (ear) = (ear) – 1, and (ear) \neq 0	—	—	—	—	—	*	*	*	—	—
DWBNZ eam, rel	3+	*6	2	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) \neq 0	—	—	—	—	—	*	*	*	—	*
INT #vct8	2	20	0	8× (c)	Software interrupt	—	—	R	S	—	—	—	—	—	—
INT addr16	3	16	0	6× (c)	Software interrupt	—	—	R	S	—	—	—	—	—	—
INTP addr24	4	17	0	6× (c)	Software interrupt	—	—	R	S	—	—	—	—	—	—
INT9	1	20	0	8× (c)	Software interrupt	—	—	R	S	—	—	—	—	—	—
RETI	1	15	0	*7	Return from interrupt	—	—	*	*	*	*	*	*	*	—
LINK #imm8	2	6	0	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	—	—	—	—	—	—	—	—	—	—
UNLINK	1	5	0	(c)	At constant entry, retrieve old frame pointer from stack.	—	—	—	—	—	—	—	—	—	—
RET ^{*8}	1	4	0	(c)		—	—	—	—	—	—	—	—	—	—
RETP ^{*9}	1	6	0	(d)	Return from subroutine	—	—	—	—	—	—	—	—	—	—
					Return from subroutine										

*1: 5 when branching, 4 when not branching

*2: 13 when branching, 12 when not branching

*3: 7 + (a) when branching, 6 + (a) when not branching

*4: 8 when branching, 7 when not branching

*5: 7 when branching, 6 when not branching

*6: 8 + (a) when branching, 7 + (a) when not branching

*7: Set to 3 × (b) + 2 × (c) when an interrupt request occurs, and 6 × (c) for return.

*8: Retrieve (word) from stack

*9: Retrieve (long word) from stack

*10: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 21 Other Control Instructions (Byte/Word/Long Word) [28 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	4	0	(c)	word (SP) \leftarrow (SP) -2, ((SP)) \leftarrow (A)	-	-	-	-	-	-	-	-	-	-
PUSHW AH	1	4	0	(c)	word (SP) \leftarrow (SP) -2, ((SP)) \leftarrow (AH)	-	-	-	-	-	-	-	-	-	-
PUSHW PS	1	4	0	(c)	word (SP) \leftarrow (SP) -2, ((SP)) \leftarrow (PS)	-	-	-	-	-	-	-	-	-	-
PUSHW rlst	2	*3	*5	*4	(SP) \leftarrow (SP) -2n, ((SP)) \leftarrow (rlst)	-	-	-	-	-	-	-	-	-	-
POPW A	1	3	0	(c)	word (A) \leftarrow ((SP)), (SP) \leftarrow (SP) +2	-	*	-	-	-	-	-	-	-	-
POPW AH	1	3	0	(c)	word (AH) \leftarrow ((SP)), (SP) \leftarrow (SP) +2	-	-	-	-	-	-	-	-	-	-
POPW PS	1	4	0	(c)	word (PS) \leftarrow ((SP)), (SP) \leftarrow (SP) +2	-	-	*	*	*	*	*	*	*	-
POPW rlst	2	*2	*5	*4	(rlst) \leftarrow ((SP)), (SP) \leftarrow (SP) +2n	-	-	-	-	-	-	-	-	-	-
JCTX @A	1	14	0	6× (c)	Context switch instruction	-	-	*	*	*	*	*	*	*	-
AND CCR, #imm8	2	3	0	0	byte (CCR) \leftarrow (CCR) and imm8	-	-	*	*	*	*	*	*	*	-
OR CCR, #imm8	2	3	0	0	byte (CCR) \leftarrow (CCR) or imm8	-	-	*	*	*	*	*	*	*	-
MOV RP, #imm8	2	2	0	0	byte (RP) \leftarrow imm8	-	-	-	-	-	-	-	-	-	-
MOV ILM, #imm8	2	2	0	0	byte (ILM) \leftarrow imm8	-	-	-	-	-	-	-	-	-	-
MOVEA RWi, ear	2	3	1	0	word (RWi) \leftarrow ear	-	-	-	-	-	-	-	-	-	-
MOVEA RWi, eam	2+	2+ (a)	1	0	word (RWi) \leftarrow eam	-	-	-	-	-	-	-	-	-	-
MOVEA A, ear	2	1	0	0	word (A) \leftarrow ear	-	*	-	-	-	-	-	-	-	-
MOVEA A, eam	2+	1+ (a)	0	0	word (A) \leftarrow eam	-	*	-	-	-	-	-	-	-	-
ADDSP #imm8	2	3	0	0	word (SP) \leftarrow (SP) +ext (imm8)	-	-	-	-	-	-	-	-	-	-
ADDSP #imm16	3	3	0	0	word (SP) \leftarrow (SP) +imm16	-	-	-	-	-	-	-	-	-	-
MOV A, brgl	2	*1	0	0	byte (A) \leftarrow (brgl)	Z	*	-	-	-	*	*	-	-	-
MOV brg2, A	2	1	0	0	byte (brg2) \leftarrow (A)	-	-	-	-	-	*	*	-	-	-
NOP	1	1	0	0	No operation	-	-	-	-	-	-	-	-	-	-
ADB	1	1	0	0	Prefix code for accessing AD space	-	-	-	-	-	-	-	-	-	-
DTB	1	1	0	0	Prefix code for accessing DT space	-	-	-	-	-	-	-	-	-	-
PCB	1	1	0	0	Prefix code for accessing PC space	-	-	-	-	-	-	-	-	-	-
SPB	1	1	0	0	Prefix code for accessing SP space	-	-	-	-	-	-	-	-	-	-
NCC	1	1	0	0	Prefix code for no flag change	-	-	-	-	-	-	-	-	-	-
CMR	1	1	0	0	Prefix code for common register bank	-	-	-	-	-	-	-	-	-	-

*1: PCB, ADB, SSB, USB, and SPB : 1 state

DTB, DPR : 2 states

*2: $7 + 3 \times (\text{pop count}) + 2 \times (\text{last register number to be popped})$, 7 when rlst = 0 (no transfer register)

*3: $29 + (\text{push count}) - 3 \times (\text{last register number to be pushed})$, 8 when rlst = 0 (no transfer register)

*4: Pop count \times (c), or push count \times (c)

*5: Pop count or push count.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 22 Bit Manipulation Instructions [21 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB A, dir:bp	3	5	0	(b)	byte (A) \leftarrow (dir:bp) b	Z	*	—	—	—	*	*	—	—	—
MOVB A, addr16:bp	4	5	0	(b)	byte (A) \leftarrow (addr16:bp) b	Z	*	—	—	—	*	*	—	—	—
MOVB A, io:bp	3	4	0	(b)	byte (A) \leftarrow (io:bp) b	Z	*	—	—	—	*	*	—	—	—
MOVB dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b \leftarrow (A)	—	—	—	—	—	*	*	—	—	*
MOVB addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b \leftarrow (A)	—	—	—	—	—	*	*	—	—	*
MOVB io:bp, A	3	6	0	2× (b)	bit (io:bp) b \leftarrow (A)	—	—	—	—	—	*	*	—	—	*
SETB dir:bp	3	7	0	2× (b)	bit (dir:bp) b \leftarrow 1	—	—	—	—	—	—	—	—	—	*
SETB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b \leftarrow 1	—	—	—	—	—	—	—	—	—	*
SETB io:bp	3	7	0	2× (b)	bit (io:bp) b \leftarrow 1	—	—	—	—	—	—	—	—	—	*
CLRB dir:bp	3	7	0	2× (b)	bit (dir:bp) b \leftarrow 0	—	—	—	—	—	—	—	—	—	*
CLRB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b \leftarrow 0	—	—	—	—	—	—	—	—	—	*
CLRB io:bp	3	7	0	2× (b)	bit (io:bp) b \leftarrow 0	—	—	—	—	—	—	—	—	—	*
BBC dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 0	—	—	—	—	—	—	*	—	—	—
BBC addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 0	—	—	—	—	—	—	*	—	—	—
BBC io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 0	—	—	—	—	—	—	*	—	—	—
BBS dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	—	—	—	—	—	—	*	—	—	—
BBS addr16:bp, rel	4	*2	0	(b)	Branch when (addr16:bp) b = 1	—	—	—	—	—	—	*	—	—	—
BBS io:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	—	—	—	—	—	—	*	—	—	*
SBBS addr16:bp, rel	3	*4	0	*5	Wait until (io:bp) b = 1	—	—	—	—	—	—	—	—	—	—
WBTS io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	—	—	—	—	—	—	—	—	—	—
WBTC io:bp															

*1: 8 when branching, 7 when not branching

*2: 7 when branching, 6 when not branching

*3: 10 when condition is satisfied, 9 when not satisfied

*4: Undefined count

*5: Until condition is satisfied

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 23 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 to 7 \leftrightarrow (A) 8 to 15	—	—	—	—	—	—	—	—	—	—
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) \leftrightarrow (AL)	—	*	—	—	—	—	—	—	—	—
EXT	1	1	0	0	byte sign extension	X	—	—	—	—	*	*	—	—	—
EXTW	1	2	0	0	word sign extension	—	X	—	—	—	*	*	—	—	—
ZEXT	1	1	0	0	byte zero extension	Z	—	—	—	—	R	*	—	—	—
ZEXTW	1	1	0	0	word zero extension	—	Z	—	—	—	R	*	—	—	—

Table 24 String Instructions [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVS	2	*2	*5	*3	Byte transfer @AH+ \leftarrow @AL+, counter = RW0	—	—	—	—	—	—	—	—	—	—
MOVSD	2	*2	*5	*3	Byte transfer @AH- \leftarrow @AL-, counter = RW0	—	—	—	—	—	—	—	—	—	—
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) - AL, counter = RW0	—	—	—	—	—	*	*	*	*	—
SCEQD	2	*1	*5	*4	Byte retrieval (@AH-) - AL, counter = RW0	—	—	—	—	—	*	*	*	*	—
FISL/FILSI	2	6m + 6	*5	*3	Byte filling @AH+ \leftarrow AL, counter = RW0	—	—	—	—	—	*	*	—	—	—
MOVSW/	2	*2	*8	*6	Word transfer @AH+ \leftarrow @AL+, counter = RW0	—	—	—	—	—	—	—	—	—	—
MOVSWI	2	*2	*8	*6	Word transfer @AH- \leftarrow @AL-, counter = RW0	—	—	—	—	—	—	—	—	—	—
MOVSWD	2	*1	*8	*7	Word retrieval (@AH+) - AL, counter = RW0	—	—	—	—	—	*	*	*	*	—
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH-) - AL, counter = RW0	—	—	—	—	—	*	*	*	*	—
SCWEQD	2	6m + 6	*8	*6	Word filling @AH+ \leftarrow AL, counter = RW0	—	—	—	—	—	*	*	—	—	—
FILSW/FILSWI	2	6m + 6	*8	*6	Word filling @AH+ \leftarrow AL, counter = RW0	—	—	—	—	—	*	*	—	—	—

m: RW0 value (counter value)

n: Loop count

*1: 5 when RW0 is 0, $4 + 7 \times (\text{RW0})$ for count out, and $7 \times n + 5$ when match occurs

*2: 5 when RW0 is 0, $4 + 8 \times (\text{RW0})$ in any other case

*3: $(b) \times (\text{RW0}) + (b) \times (\text{RW0})$ when accessing different areas for the source and destination, calculate (b) separately for each.

*4: $(b) \times n$

*5: $2 \times (\text{RW0})$

*6: $(c) \times (\text{RW0}) + (c) \times (\text{RW0})$ when accessing different areas for the source and destination, calculate (c) separately for each.

*7: $(c) \times n$

*8: $2 \times (\text{RW0})$

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 25 2-byte Instruction Map [Byte 1 = 6 FH]

	00	10	20	30	40	50	60	70	80	90	A0	B0	C0	D0	E0	F0
+0	MOV A, DTB	MOV DTB, A	MOVX A, @RL0 + d8	MOV @RL0 + d8, A	MOV A, @RL0 + d8											
+1	MOV A, ADB	MOV ADB, A														
+2	MOV A, SSB	MOV SSB, A	MOVX A, @RL1 + d8	MOV @RL1 + d8, A	MOV A, @RL1 + d8											
+3	MOV A, USB	MOV USB, A														
+4	MOV A, DPR	MOV DPR, A	MOVX A, @RL2 + d8	MOV @RL2 + d8, A	MOV A, @RL2 + d8											
+5	MOV A, @A	MOV @AL, AH														
+6	MOV A, PCB	MOVX A, @A	MOVX A, @RL3 + d8	MOV @RL3 + d8, A	MOV A, @RL3 + d8											
+7	ROL A	RORC A														
+8				MOVW @RL 0 + d8, A	MOVW A, @RL0 + d8			MUL A								
+9								MULW A								
+A				MOVW @RL 1 + d8, A	MOVW A, @RL1 + d8			DIVU A								
+B																
+C	LSLW A, R0	LSLL A, R0	LSL A, R0	MOVW @RL 2 + d8, A	MOVW A, @RL2 + d8											
+D	MOVW A, @A	MOVW @AL, AH	NRML A, R0													
+E	ASRW A, R0	ASRL A, R0	ASR A, R0	MOVW @RL 3 + d8, A	MOVW A, @RL3 + d8											
+F	LSRW A, R0	LSRL A, R0	LSR A, R0													

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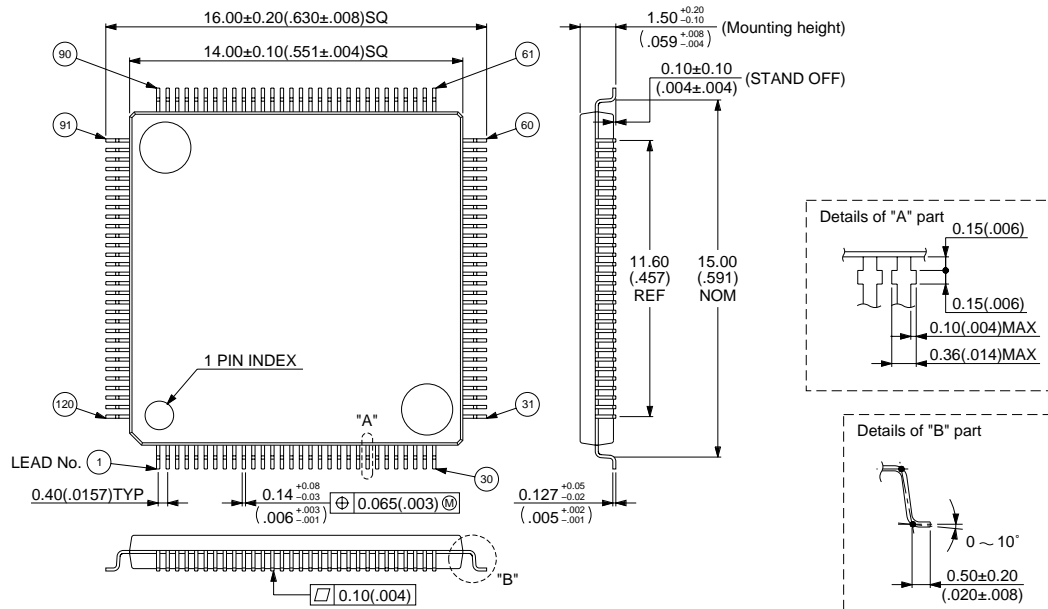
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F574/APFF MB90574PFF MB90573PFF	120-pin Plastic LQFP (FPT-120P-M05)	
MB90F574/APFV MB90574/APFV MB90573PFV	120-pin Plastic QFP (FPT-120P-M13)	
MB90F57APMT MB90574APMT	120-pin Plastic LQFP (FPT-120P-M21)	

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■ PACKAGE DIMENSIONS

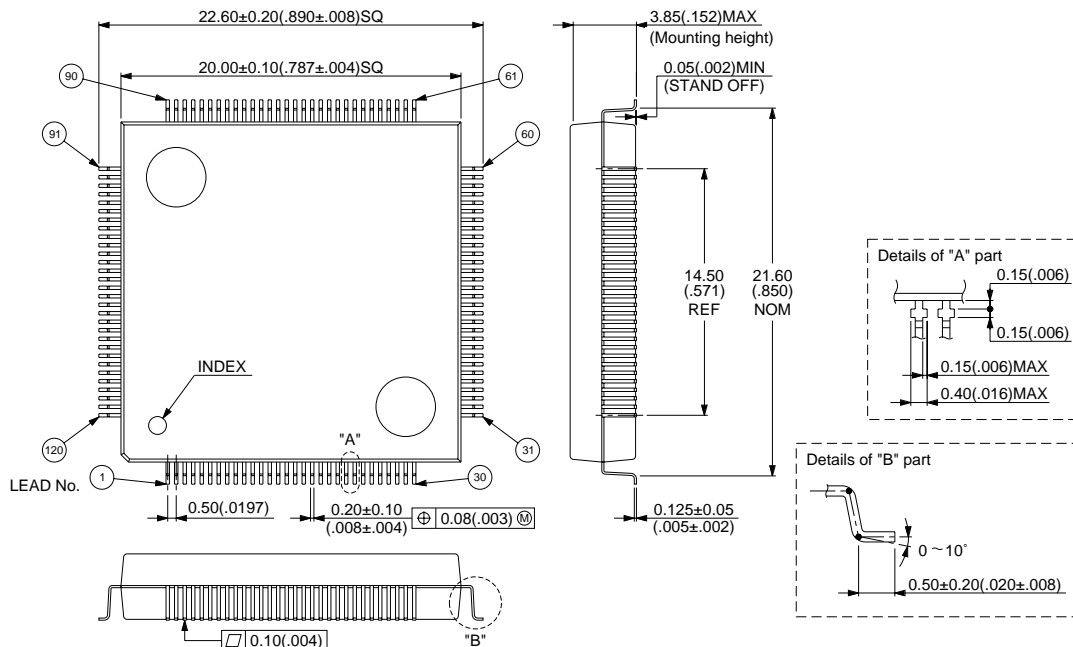
120-pin plastic LQFP
(FPT-120P-M05)



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Dimensions in mm (inches)

120-pin plastic QFP
(FPT-120P-M13)

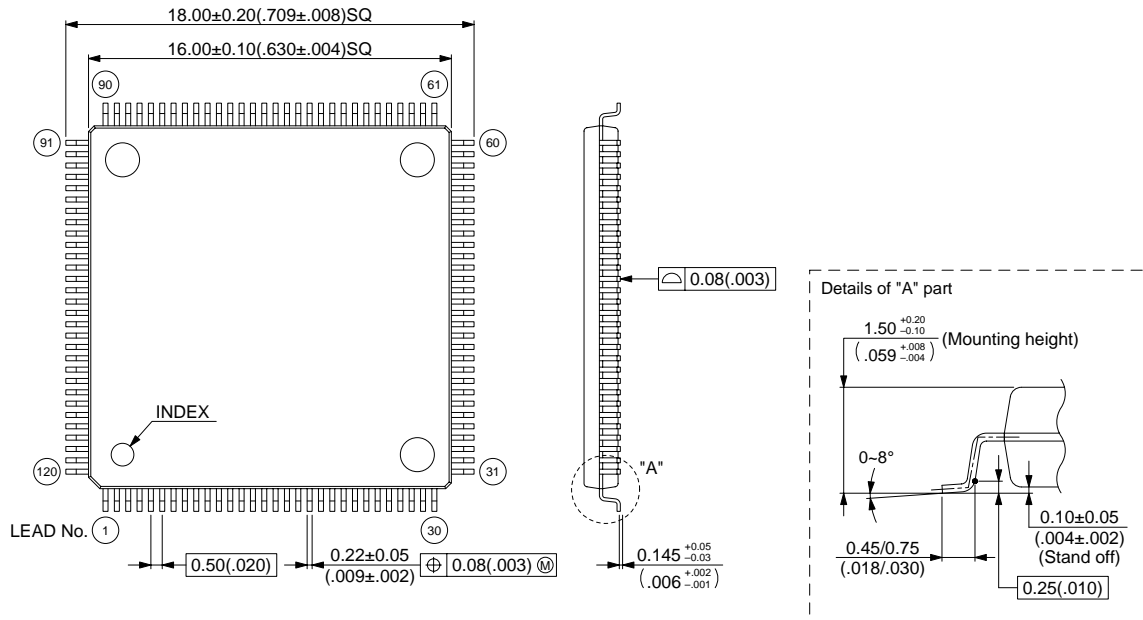


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Dimensions in mm (inches)

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120-pin plastic LQFP
(FPT-120P-M21)



Dimensions in mm (inches)

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